Digital Signal Processing in RF Applications

Part I

Thomas Schilcher

Paul Scherrer Institut (PSI)
What are RF applications?

- any application which measures properties of an RF field (amplitude, phase, frequency, ...);
  typical frequencies in accelerators: MHz – tens of GHz

- applications which process the measured quantities to control and regulate RF fields
  (feedback and feedforward)
Typical RF applications

Accelerators:

- CW / pulsed machines
- linear / circular machines
- electron/hadron/ion accelerators
- normal-/superconducting RF systems

Application areas (examples):

- cavity field loops (amplitude and phase)
- klystron loops (amplitude and phase)
- tuner loops (cavity tuning)
- radial and phase loops (circular machines)
- “RF gymnastics” (bunch splitting and merging)
## Why digital RF applications?

<table>
<thead>
<tr>
<th></th>
<th><strong>Digital</strong></th>
<th><strong>Analogue</strong></th>
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<tr>
<td><strong>Implementation</strong></td>
<td>Learning curve + s/w effort</td>
<td>Easier/known</td>
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<tr>
<td><strong>Latency</strong></td>
<td>Longer</td>
<td>Short</td>
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<tr>
<td><strong>DAQ/control</strong></td>
<td>I/Q sampling (also direct) or DDC</td>
<td>Ampli/phase, IF downconversion</td>
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<tr>
<td><strong>Algorithms</strong></td>
<td>Sophisticated, State machines, exception handling...</td>
<td>Simple, Linear, time-invariant (ex: PID)</td>
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<tr>
<td><strong>Multi-user</strong></td>
<td>Full</td>
<td>Limited</td>
</tr>
<tr>
<td><strong>Remote control &amp; diagnostics</strong></td>
<td>Easy, often no additional h/w</td>
<td>Difficult, extra h/w</td>
</tr>
<tr>
<td><strong>Flexibility / reconfigurability</strong></td>
<td>High (easier upgrades)</td>
<td>Limited</td>
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<tr>
<td><strong>Drift/tolerance</strong></td>
<td>No drifts, repeatability</td>
<td>Drift (temperature), components tolerance</td>
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<tr>
<td><strong>Transport distance without distortion</strong></td>
<td>Longer</td>
<td>Short</td>
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<tr>
<td><strong>Radiation sensitivity</strong></td>
<td>High</td>
<td>Small</td>
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*M. E. Anoletta “Digital LLRF” EPAC’06*
Key components of digital RF applications

RF signal → signal conditioning / down conversion → digitization
amp./phase/I/Q detection

accelerator/plant → RF signal → vector modulator / up conversion / amplification
(feedback applications) → digital signal processing / algorithms
monitoring / control system

LLRF looks very similar to many other applications, e.g. diagnostics (bunch-by-bunch feedback, position monitoring, …)

for feedback systems: ultimate error is dominated by the measurement process
(systematic error, accuracy, linearity, repeatability, stability, resolution, noise)
Outline

1. signal conditioning / down conversion
2. detection of amp./phase by digital I/Q sampling
   - I/Q sampling
   - non I/Q sampling
   - digital down conversion (DDC)
3. upconversion
4. algorithms in RF applications
   - feedback systems
   - adaptive feed forward
   - system identification
Outline

1. **signal conditioning / down conversion**
   - detection of amp./phase by digital I/Q sampling
     - I/Q sampling
     - non I/Q sampling
     - digital down conversion (DDC)

2. **upconversion**

3. **algorithms in RF applications**
   - feedback systems
   - adaptive feed forward
   - system identification
Signal conditioning / down conversion

Why down conversion of the RF signal?

- ADC speeds are limited.
  It is not reasonable/possible today to digitize high-frequency carriers directly. ($f > 500$ MHz)

- ADC dynamic range is limited.
  
  
<table>
<thead>
<tr>
<th>Bit Depth</th>
<th>Dynamic Range</th>
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<tbody>
<tr>
<td>10 bit</td>
<td>60 dB</td>
</tr>
<tr>
<td>12 bit</td>
<td>72 dB</td>
</tr>
<tr>
<td>14 bit</td>
<td>84 dB</td>
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  → often better: use analogue circuits in conjunction with the ADC to implement automated gain control (AGC) functions to ensure that this range is best used

- ADC clock and aperture jitter become critical at high frequencies (especially for undersampling schemes)

→ RF mixers are essential for digital high frequency applications
**RF mixer (ideal)**

\[ y_{RF}(t) = A_{RF} \cdot \sin(\omega_{RF}t + \varphi_{RF}) \]

\[ f_{RF} \quad f_{IF} \quad f_{LO} \]

\[ y_{IF}(t) = y_{RF}(t) \cdot y_{LO}(t) \]

\[ y_{LO}(t) = A_{LO} \cdot \cos(\omega_{LO}t + \varphi_{LO}) \]

**m**\_\(\text{ixer: linear time varying circuit, non-linear circuit (diodes...)}\)

\[ \Rightarrow y_{IF}(t) = \frac{1}{2} A_{LO} A_{RF} \cdot \left[ \sin[(\omega_{RF} - \omega_{LO})t + (\varphi_{RF} - \varphi_{LO})] \right. \]

\[ + \left. \sin[(\omega_{RF} + \omega_{LO})t + (\varphi_{RF} + \varphi_{LO})] \right] \]

**lower sideband**

\(\text{upper sideband}\)

\(\Rightarrow \text{even ideal mixers produce two sidebands}\)
RF mixer (ideal)

- Ideal mixer: output is the multiplication of the two input signals

- Down conversion:
  RF, LO are high frequency inputs
  IF: lower intermediate frequency output

- Up conversion:
  IF is input, RF is output
RF mixer (ideal)

down conversion:
\[ y_{IF}(t) = \frac{1}{2} A_{LO} A_{RF} \cdot \left( \sin[(\omega_{RF} - \omega_{LO}) t + (\varphi_{RF} - \varphi_{LO})] + \sin[(\omega_{RF} + \omega_{LO}) t + (\varphi_{RF} + \varphi_{LO})] \right) \]

low pass filtering the upper sideband:
\[ \Rightarrow y_{IF}(t) = A_{IF} \cdot \sin \left( \omega_{IF} t + \varphi_{IF} \right) \]

- \[ \omega_{IF} = \omega_{RF} - \omega_{LO} \]
- \[ A_{IF} = \frac{1}{2} A_{LO} A_{RF} \sim A_{RF} \text{ with constant } A_{LO} \]
- \[ \varphi_{IF} = \varphi_{RF} - \varphi_{LO} \sim \varphi_{RF} \text{ with constant } \varphi_{LO} \]

**important properties:**

- phase changes/jitter are conserved during down conversion, e.g. \( 1^\circ \) @ \( f_{RF} = 1.5 \text{ GHz} \) ↔ \( 1^\circ \) @ \( f_{IF} = 50 \text{ MHz} \)

- comparison: sampling IF or RF (direct sampling)?
  timing jitter results in different phases!
  (e.g. \( 10 \text{ ps} \) @ \( 500 \text{ MHz} \) → \( 1.8^\circ \); \( 10 \text{ ps} \) @ \( 50 \text{ MHz} \) → \( 0.18^\circ \))

**tougher requirements for direct RF sampling!**
RF mixer (real)

real mixers = non linear devices
- many undesired harmonics in frequency spectrum
- non-linearities in IF signal

I-V curve of a diode

I = I_0 (e^{V/V_T} - 1)

\[ \Delta I = I_0 e^{V/V_T} \left( \frac{\Delta V}{V_T} + \frac{1}{2} \left( \frac{\Delta V}{V_T} \right)^2 + \frac{1}{6} \left( \frac{\Delta V}{V_T} \right)^3 + \ldots \right) \]

filtering the output of a mixer might be necessary
- take care about the introduced group delay by the filter

trade off!
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   - I/Q sampling
   - non I/Q sampling
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3. upconversion
4. algorithms in RF applications
   - feedback systems
   - adaptive feed forward
   - system identification
Amplitude and phase detection

- direct amplitude phase detectors

- analogue IQ detection

- digital IQ sampling / Digital Down Conversion (DDC)
RF vector representation

representation of any sinusoidal RF signal: phasor
(assumption: we measure the vertical component with ADC)

\[
y(t) = A \cdot \sin(\omega t + \varphi_0)
\]

\[
y(t) = A \cos \varphi_0 \sin \omega t + A \sin \varphi_0 \cos \omega t
\]

\[
\Rightarrow I = :I = I = A \cdot \cos \varphi_0
\]

\[
Q = :Q = A \cdot \sin \varphi_0
\]

definition:
positive frequencies
\leftrightarrow counterclockwise rotating phasor
IQ sampling (1)

**goal:** monitor amplitude/phase ($A/\varphi_0$) variations of incoming RF/IF signal

Possible also to monitor I/Q at a reference time (reference phase)

"process" sampled I/Q values for comparison, i.e. rotate phasor back to reference phasor if phase advance between sampling is well known
IQ sampling (2)

sampling of RF/IF freq.: \[ f_s = 4 \cdot f \]

(i.e. 90° phase advance between two samples)

\[
y(t) = I \cdot \sin \omega t + Q \cdot \cos \omega t
\]

\[
I = A \cdot \cos \varphi_0
\]

\[
Q = A \cdot \sin \varphi_0
\]

\[
\begin{align*}
\omega t_0 &= 0 : & y(t_0) &= Q \\
\omega t_1 &= \pi/2 : & y(t_1) &= I \\
\omega t_2 &= \pi : & y(t_2) &= -Q \\
\omega t_3 &= 3\pi/2 : & y(t_3) &= -I
\end{align*}
\]
IQ sampling (3)

- build up I/Q vector based on two successive samples
- rotate corresponding I/Q vector by -90° / -180° / -270° in order to compare to initial I/Q values

\[
\begin{align*}
y_0 &= y(t_0) = Q \\
y_1 &= y(t_1) = I \\
y_2 &= y(t_2) = -Q \\
y_3 &= y(t_3) = -I
\end{align*}
\]

rotation matrix with angle \( \Delta \phi \):
\[
\begin{pmatrix}
\cos \Delta \phi & -\sin \Delta \phi \\
\sin \Delta \phi & \cos \Delta \phi
\end{pmatrix}
\]

\[
\begin{align*}
t_0 : \begin{pmatrix} 1 & 0 \\ 0 & 1 \end{pmatrix} \cdot \begin{pmatrix} y_1 \\ y_0 \end{pmatrix} &= \begin{pmatrix} y_1 \\ y_0 \end{pmatrix} = \begin{pmatrix} I \\ Q \end{pmatrix}_t_0 \\
t_1 : \begin{pmatrix} 0 & 1 \\ -1 & 0 \end{pmatrix} \cdot \begin{pmatrix} y_2 \\ y_1 \end{pmatrix} &= \begin{pmatrix} y_1 \\ -y_2 \end{pmatrix} = \begin{pmatrix} I \\ Q \end{pmatrix}_t_1 \\
t_2 : \begin{pmatrix} -1 & 0 \\ 0 & -1 \end{pmatrix} \cdot \begin{pmatrix} y_3 \\ y_2 \end{pmatrix} &= \begin{pmatrix} -y_3 \\ -y_2 \end{pmatrix} = \begin{pmatrix} I \\ Q \end{pmatrix}_t_2 \\
t_3 : \begin{pmatrix} 0 & -1 \\ 1 & 0 \end{pmatrix} \cdot \begin{pmatrix} y_4 \\ y_3 \end{pmatrix} &= \begin{pmatrix} -y_3 \\ y_4 \end{pmatrix} = \begin{pmatrix} I \\ Q \end{pmatrix}_t_3
\end{align*}
\]

⇒ I/Q processing with sampling frequency \( f_S \)
IQ sampling (4)

**general:** \( f_s / f_{IF} = m, \quad m : \text{integer} \)

Phase advance between consecutive samples: \( \Delta \varphi = \frac{2\pi}{m} \)

1. relation between measured amplitudes and I/Q

\[
\begin{pmatrix}
  I_n \\
  Q_n
\end{pmatrix} = \frac{1}{\sin \Delta \varphi} \cdot \begin{pmatrix} 1 & -\cos \Delta \varphi \\ 0 & \sin \Delta \varphi \end{pmatrix} \cdot \begin{pmatrix} y_{n+1} \\
  y_n
\end{pmatrix}
\]

2. rotation of \( \begin{pmatrix} I_n \\
  Q_n \end{pmatrix} \) to \( \begin{pmatrix} I_0 \\
  Q_0 \end{pmatrix} = \begin{pmatrix} y_i \\
  y_0 \end{pmatrix} \) with angle \( -n\Delta \varphi \):

\[
\begin{pmatrix}
  I_0 \\
  Q_0
\end{pmatrix} = \frac{1}{\sin \Delta \varphi} \cdot \begin{pmatrix} \cos n\Delta \varphi & -\cos(n+1)\Delta \varphi \\ -\sin n\Delta \varphi & \sin(n+1)\Delta \varphi \end{pmatrix} \cdot \begin{pmatrix} y_{n+1} \\
  y_n
\end{pmatrix}
\]

3. rotation of \( \begin{pmatrix} I_0 \\
  Q_0 \end{pmatrix} \) to \( \begin{pmatrix} I \\
  Q \end{pmatrix} \) with angle \( -\varphi \):

\[
\begin{pmatrix}
  I \\
  Q
\end{pmatrix} = \frac{1}{\sin \Delta \varphi} \cdot \begin{pmatrix} \cos (\varphi + n\Delta \varphi) & -\cos (\varphi + (n+1)\Delta \varphi) \\ -\sin (\varphi + n\Delta \varphi) & \sin (\varphi + (n+1)\Delta \varphi) \end{pmatrix} \cdot \begin{pmatrix} y_{n+1} \\
  y_n
\end{pmatrix}
\]
IQ sampling – potential problems (1)

- DC offsets of carrier frequency
- samples are not exactly 90° apart (e.g. due to ADC clock jitter)
  - ripple on I/Q values with freq. of carrier (e.g. $f_{IF}$)

- choosing phase advances “far” away from 90° can worsen signal to noise ratio

\[
\begin{pmatrix}
I_0 \\
Q_0
\end{pmatrix} = \begin{pmatrix}
\frac{1}{\sin \Delta \varphi} \\
\sin \Delta \varphi
\end{pmatrix} \begin{pmatrix}
\cos n \Delta \varphi & -\cos(n + 1) \Delta \varphi \\
-\sin n \Delta \varphi & \sin(n + 1) \Delta \varphi
\end{pmatrix} \begin{pmatrix}
y_{n+1} \\
y_n
\end{pmatrix}
\]

“easily” detectable errors in IQ demodulation
IQ sampling – potential problems (2)

- differential non-linearities of ADCs
- non-linearities of mixers
  - generate high harmonics of input carrier
  - odd harmonics of carrier frequency are not distinguishable from carrier by IQ detection

example:
IF fundamental with 20% of 3rd harmonic component

if input phase and amplitude changes, the distortion changes and can corrupt the measurement
Non-IQ sampling

recall: \[ y(t) = I \cdot \sin \omega t + Q \cdot \cos \omega t \]

choose sampling frequency \( f_S \) and IF frequency \( f_{IF} \) such that:

\[ N \cdot T_s = M \cdot T_{IF} \quad f_s = \frac{N}{M} \cdot f_{IF} \quad N, M: \text{ integers} \]

\( N \) samples in \( M \) IF periods

\( \longrightarrow \) phase advance between two samples: \[ \Delta \varphi = \omega_{IF} T_s = 2\pi \frac{T_s}{T_{IF}} = 2\pi \frac{M}{N} \]

\( \longrightarrow \) sampling “whole” IF sinusoidal signal if \( M, N \) are properly chosen

example: \( M=3 \) (IF periods), \( N=25 \)

\[
\begin{align*}
    y_0 &= I \cdot \sin \varphi_0 + Q \cdot \cos \varphi_0 \\
    y_1 &= I \cdot \sin \varphi_1 + Q \cdot \cos \varphi_1 \\
    y_2 &= I \cdot \sin \varphi_2 + Q \cdot \cos \varphi_2 \\
    \vdots \\
    y_{(N-1)} &= I \cdot \sin \varphi_{(N-1)} + Q \cdot \cos \varphi_{(N-1)}
\end{align*}
\]

where \( \varphi_i = i \cdot \Delta \varphi = i \cdot 2\pi \frac{M}{N} \)

\( \longrightarrow \) overestimated system of linear equations

\( \longrightarrow \) can be solved by least mean square algorithm
Non-IQ sampling (2)

least mean square algorithm: minimize with respect to $I,Q$

$$f(I, Q) = \sum_{i=0}^{N-1} \left( I \cdot \sin \varphi_i + Q \cdot \cos \varphi_i - y_i \right)^2$$

$$\frac{\partial f}{\partial I} = 0, \quad \frac{\partial f}{\partial Q} = 0$$

$I = 2N \cdot \sum_{i=0}^{N-1} y_i \cdot \sin(i \cdot \Delta \varphi)$

$Q = 2N \cdot \sum_{i=0}^{N-1} y_i \cdot \cos(i \cdot \Delta \varphi)$

if $N \cdot T_s = M \cdot T_{IF}$

(sin and cos can be pre-calculated and stored in look-up tables)

$$\varphi_i = i \cdot \Delta \varphi = i \cdot 2\pi \frac{M}{N}$$
Non-IQ sampling (3)

Aliasing of harmonics:

- errors from DC offsets, clock jitter, ADC quantization, noise reduced
- but more latency due to sampling $M \cdot f_{IF}$ periods
- trade-off between noise reduction and linearity improvement and low latency

Choose $M, N$ properly!
Digital Down Conversion (DDC)

(sometimes referred to as “Digital Drop Receiver” (DDR))

Goal: shift the digitized band limited RF or IF signal from its carrier down to baseband

Example: \( f_{IF} = 40 \text{ MHz} \)
\( f_s = 100 \text{ MHz} \) (oversampling)
Signal BW = 1 MHz
Output sample rate of 2.5 MHz is fine!

- reduce the amount of required subsequent processing of the signal without loss of any of the information carried by the IF signal

- filtering and data reduction!

- Implementation on FPGA, DSP or ASIC
- Two classes of DDCs:
  - Narrowband (decimation \( R \geq 32 \), \( \rightarrow \) CIC filter [Cascaded Integrator Comb])
  - Wideband (decimation \( R < 32 \), \( \rightarrow \) FIR / multi-rate FIR filters)
DDC (2)

inside DDC: three major sections

- Local Oscillator (Numerical Controlled Oscillator, NCO)
- Mixer (digital)
- Decimating Low Pass Filter (LPF)

DDC building blocks:
- NCO: direct digital frequency synthesizer (DDS)
  sine and cosine lookup table
- digital mixers: “ideal” multipliers → two output frequencies
  (sum and difference freq. signals)
- decimating low pass (anti alias) filter (often implemented as CIC and FIR)
DDC building block: NCO

NCO functionality:

- **phase accumulator** → calculate new phase @ $f_S$ with phase advance defined by tuning word. (NCO clock: sample rate $f_S$)
- **convert phase to amplitude**
  (often done in ROM based sine lookup tables; either one full sin wave is stored or only a quarter with some math on the pointer increment)
- phase accumulator overflow → wrap around in circular lookup table

NCO advantages:

- tuning word is programmable
  - frequencies up to nearly $f_S/2$ (Nyquist) possible
- extremely fast “hopping speed” in tuning output frequency, phase-continuous frequency hops with no over/undershoot or analog-related loop settling time anomalies.
addendum: Direct Digital Synthesis (DDS)

DDS properties:
- produce an analog waveform by generating a time-varying signal in digital form
- size of lookup table (phase to amp. conv.) is determined by:
  - number of table entries
  - bit width of entries (determines amplitude output resolution)
- output frequency: 
  \[ f_{out} = M \cdot \frac{f_{CLK}}{2^N} \]  
  \( M \): tuning word, \( N \): length in bits of phase accumulator

example: \( N=32 \) bit; \( f_S=50 \) MHz \( \rightarrow \) \( df=12 \) mHz

**but:** do we need \( 2^N \) (8 bit entries \( \rightarrow \) 4 GByte!) entries in lookup table?
Direct Digital Synthesis (2)

Phase truncation:

- in order to save memory in lookup table:
  - truncate phase before the lookup table!
  
  *example*: $N=32$: keep only upper most 12 bits, truncate lower 20 bits

- implications:
  - introduce phase error which is periodic in time
  - result in amplitude errors during phase to amplitude conversion

  phase truncation spurs

Output precompensation:

- $\sin(X)/X$ rolloff response due to DAC output spectrum which is quite significant
- precompensate output before DAC with inverse sinc filter
DDC building block: Cascaded Integrator Comb Filter (CIC)  
(introduced by Eugene Hogenauer, 1981)

- computationally efficient implementations of narrowband low pass filters (no multipliers needed!)
- multi-rate filter (decimation/interpolation)

basic elements:

\[ y[n] = y[n-1] + x[n] \]
\[ H_I(z) = \frac{1}{1 - z^{-1}} \]

\[ y[n] = x[n] - x[n - D] \]
\[ H_C(z) = 1 - z^{-D} \]
CIC filter (2)

Filter structure for decimating CIC:

\[ H_I(z) = \left(1 - z^{-RD}\right)^M \]

Filter structure for interpolating CIC:

\[ H_C(z) = 1 - z^{-RD} \]

D: differential delay

Reference sampling rate for transfer function: always higher freq.

Basic comb filter (referenced to the high input sample rate):

\[ H(z) = \left( H_I \right)^M \left( H_C \right)^M = \frac{(1 - z^{-RD})^M}{(1 - z^{-1})^M} = \left( \sum_{k=0}^{RD-1} z^{-k} \right)^M \]

FIR filter! (stable)
How to understand CIC?

example: decimating CIC (1st order) with integer decimation factor R

CIC: originate from the concept of a recursive running-sum filter (efficient form of a non-recursive moving average filter [boxcar filter])

boxcar filter, length $N$: (moving average)

$$y[n] = \frac{1}{N} \left( x[n] + x[n-1] + \cdots + x[n-N+1] \right)$$

$$H(z) = \frac{1}{N} \left( 1 + z^{-1} + \cdots + z^{-(N-1)} \right) = \frac{1}{N} \sum_{k=0}^{N-1} z^{-k} = \frac{1}{N} \frac{1 - z^{-N}}{1 - z^{-1}}$$

geometric sum
How to understand CIC (2)

recursive running-sum:
(alternate implementation of boxcar filter)

\[ y[n] = y[n-1] + \frac{1}{N} (x[n] - x[n-N]) \]

\[ w[n] = z^{-1} w[n] + x[n] \]
\[ y[n] = \frac{1}{N} \left( w[n] + z^{-N} w[n] \right) \]

transfer function:
\[ H(z) = \frac{1}{N} \frac{1 - z^{-N}}{1 - z^{-1}} \]

in many applications: boxcar followed by decimation \( R=N \)

boxcar/recursive running-sum filters have the same transfer function as a 1\textsuperscript{st} order CIC (except: 1/N gain; general diff. delay \( D \))

compare with 1\textsuperscript{st} order CIC:
\[ H(z) = \frac{1}{N} \frac{1 - z^{-RD}}{1 - z^{-1}} \]
RF applications

CIC properties

- **applications:**
  - anti-aliasing filtering prior to decimation
  - typically employed in applications that have a large excess sample rate.
    → system sample rate is much larger than the bandwidth occupied by the signal
    (remember example: \( f_{IF} = 40 \text{ MHz} \), \( f_s = 100 \text{ MHz} \), signal BW = 1 MHz)

- **resources:** uses additions and subtractions only

- **frequency response:** evaluate \( H(z) \) at \( z = e^{i\omega T_s} = e^{i2\pi \frac{f}{f_s}} \)

\[
|H(e^{i\omega T_s})| = \left| \frac{\sin(\pi RD \frac{f}{f_s})}{\sin(\pi \frac{f}{f_s})} \right|^M
\]

frequency response with respect to the output frequency \( f_0 = \frac{f_s}{R} \)

\[
|H(f)| = \left| \frac{\sin(\pi D \frac{f}{f_0})}{\sin(\pi \frac{f}{R f_0})} \right|^M
\]

- design parameter \( D \) determines locations of zeros:
  \[
f = k \cdot \frac{f_0}{D} \] (\( k: \text{ integer} \))
**CIC properties (2)**

- **DC gain:**
  net gain of CIC at DC: \((RD)^M\)
  
  \[
  \lim_{f \to 0} |H(f)| = (RD)^M
  \]

  → Each additional integrator must add another bits width of \((RD)\) for each stage
  (implementation with two's complement (nonsaturating) arithmetic due to overflows at each integrator)

- **frequency response:** \((M: \text{number of CIC stages}, D: \text{differential delay})\)

  ![Plot of relative frequency response](image)
  
  **important characteristic:** shape of the filter response changes very little as a function of the decimation ratio \(R\)
CIC properties (3)

- to improve alias rejection
  - increase number of CIC stages ($M$)

**but:**
- this increases passband droop
- droop is frequently corrected using an additional (non-CIC-based) stage of filtering

**compensation filter**

*decimator:* after CIC at reduced rate;

*interpolator:* precompensated before CIC

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CAS, Sigtuna, Sweden
DSP – Digital Signal Processing
T. Schilcher

06 June 2007

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RF applications
DDC or IQ demodulation?

**DDC**
- long group delay (depending on clock speed and number of taps in the CIC/FIR filters)
- very flexible (NCO can follow $f_{IF}$ over a broad range)
- data reduction and good S/N ratio

**IQ demodulation**
- low latency, simple implementation
- $f_s$ is fixed to IF
- sensitive to clock jitter and non-linearities
- non-IQ sampling provides better S/N ratio on cost of latency

- applications with large varying IF, need for good S/N ration and reasonable latency
- feedback applications with fixed IF and ultra-short latency
Examples for DDC and IQ demodulation

**DDC**
- super conducting cavity field (amplitude)

\[ f_{IF} = 13.54 \text{ MHz} \]
\[ f_S = 54.17 \text{ MHz} \]
\[ f_{CLK(\text{FPGA})} = 75 \text{ MHz} \]
5 stage CIC+ 21 tap FIR

delay: 25 clk cycles

\[ S/N \text{ improvement by factor } \sim 20 \]

**IQ demodulation**
- super conducting cavity field (amplitude)

\[ f_{IF} = 250 \text{ kHz} \]
\[ f_S = 1 \text{ MHz} \]
\[ f_{CLK(\text{FPGA})} = 75 \text{ MHz} \]
delay: 4 clk cycles

G. Castello (FNAL)
Outline

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Up conversion – vector modulator

- RF signal: split into two branches, 90° phase shift (sin, cos)
- Block diagram:

\[
RF_{out}(t) = I \cdot A_{RF} \cdot \sin \omega t + Q \cdot A_{RF} \cdot \cos \omega t
\]

\[
= A_{out} \cdot \sin(\omega t + \varphi_0)
\]

\[
A_{out} = A_{RF} \sqrt{I^2 + Q^2} \quad \varphi_0 = \arctan \left( \frac{Q}{I} \right)
\]

- Mixer operated as amplitude control elements
  - Any phase and amplitude of carrier can be generated

<table>
<thead>
<tr>
<th>Pure amplitude modulation:</th>
<th>Pure phase modulation:</th>
</tr>
</thead>
<tbody>
<tr>
<td>( I(t) = A_0(t) \cdot \cos \varphi_0 )</td>
<td>( I(t) = A_0 \cdot \cos \varphi_0(t) )</td>
</tr>
<tr>
<td>( Q(t) = A_0(t) \cdot \sin \varphi_0 )</td>
<td>( Q(t) = A_0 \cdot \sin \varphi_0(t) )</td>
</tr>
</tbody>
</table>
Vector modulator

- **homodyne upconversion** (direct upconversion, baseband upconversion):

  ![Homodyne Upconversion Diagram]

- **heterodyne upconversion** (IF upconversion)

  - **double sideband modulator**
    ![Double Sideband Modulator Diagram]
  - **single sideband modulator** (phasing method)
    ![Single Sideband Modulator Diagram]
Vector modulator

practical problems (homodyne vec. mod.): 1st order sources of errors

- offsets at mixer inputs
- two channels not exactly 90° apart
- gains of two RF paths and I/Q drives not exactly the same

- carrier leakage
- I / Q skew
- I / Q imbalance errors
Vector modulator – digital predistortion

**I/Q skew compensation**

RF output with skew:

\[
RF_{out}(t) = I_{out} \cdot A_{RF} \cdot \sin \omega t + Q_{out} \cdot A_{RF} \cdot \cos(\omega t - \varphi_S)
\]

\[
RF_{out}(t) = (I_{out} + Q_{out} \sin \varphi_S) \cdot A_{RF} \sin \omega t + Q_{out} \cos \varphi_S \cdot A_{RF} \cos \omega t
\]

predistortion of I/Q signal:

\[
\begin{pmatrix}
I_{out} \\
Q_{out}
\end{pmatrix} = \frac{1}{\cos \varphi_S} \begin{pmatrix}
\cos \varphi_S & -\sin \varphi_S \\
0 & 1
\end{pmatrix} \begin{pmatrix}
I_{in} \\
Q_{in}
\end{pmatrix}
\]

**gain/offset compensation**

define individual gain scaling factors and offset compensation constants for I/Q; pre-scale I/Q digitally before applying to vector modulator
example of I/Q skew compensation: **RF gun control for FLASH**
boundary condition: no field probe to detect field in RF cavity
predistortion: adjust for skew and for gain imbalance

**setup:**

**before vec. mod. linearization:**

- 8% variation during phase shifts of 360°

**after vec. mod. linearization:**

- 2% variation during phase shifts of 360°

**W. Koprek (DESY)**