LLRF with direct sampling

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USPAS 2017 Low

New LLRF Control System at LNL

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***Abstract*—The Low-level Radio Frequency (LLRF) control system for linear accelerator at Legnaro National Laboratories (LNL) of INFN is being upgraded by a new digital Radio Frequency (RF) controller. This controller is critical to keep phase, amplitude and frequency stability of the RF field in Quarter Wave Resonator (QWR) cavities of the linear accelerator. These cavities work in superconducting condition. The resonance frequency of low beta cavities is 80 MHz, while medium and high beta cavities resonate at 160 MHz. Each RF controller can control at the same time eight different cavities. The RF signals picked-up from the cavities are sampled by RF ADCs. The digitized signals are fed into a field programmable gate array (FPGA) which implements the control loop. The signals processed by the FPGA are in-phase/quadrature modulated and sent to power amplifiers and hence to the cavities. The main feature of the new control system is an all-digital control loop that originates from direct sampling of the antenna RF signal. In-phase and quadrature components are obtained by a suitable choice of the undersampling frequency, while control of the field and phase in the cavity is based on a digital Complex Phase Modulator (CPM). This paper presents the FPGA firmware, the acquisition techniques and the performances of the new RF controller.**

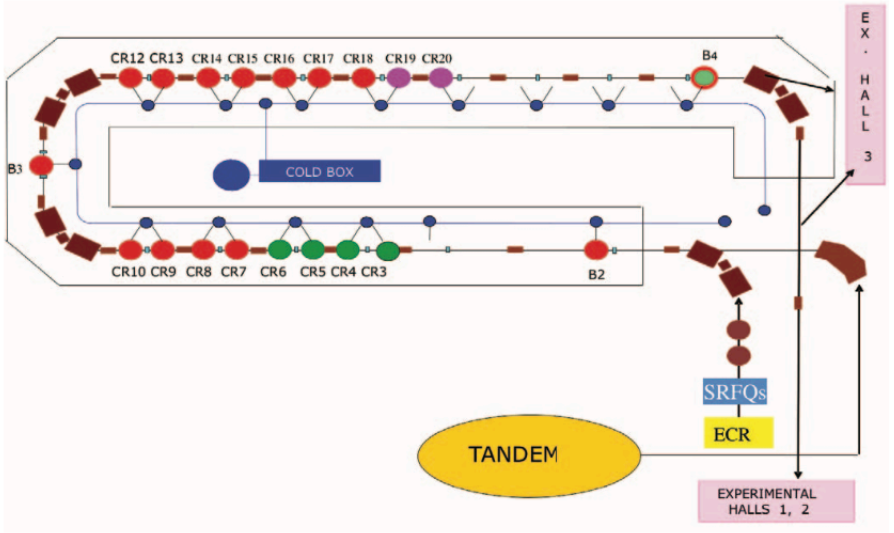


Fig. 1. Layout of ALPI

The LLRF control system plays an important role in modem accelerators. By stabilizing the phase, the amplitude and the frequency of RF field cavity, this system ensures an optimum energy gain of the accelerated beam. Hence the accelerating gradient and the phase stability has to respect tight require-

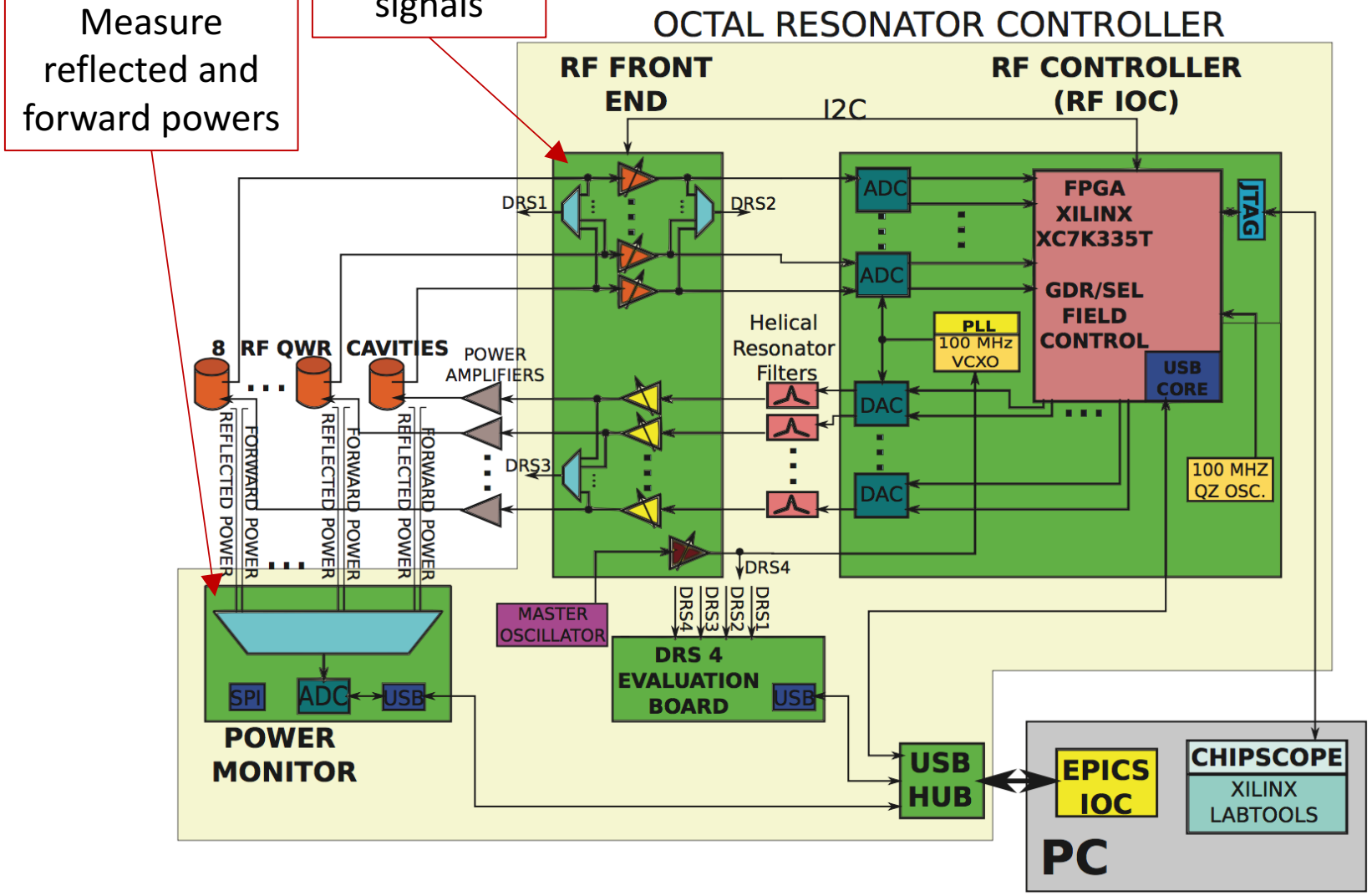
Description

- Quarter Wave Resonator (QWR) cavities, with resonance frequencies of 80 MHz and 160 MHz
- RF Controller can control 8 cavities
- The RF signals picked- up from the cavities are sampled by RF ADCs
- Control loop is implemented on a FPGA
- The main perturbations are cause by microphonics [Hz to kHz] (pressure variations in helium, temperature, mechanical vibrations, change in cavity resonance by currents/charges).

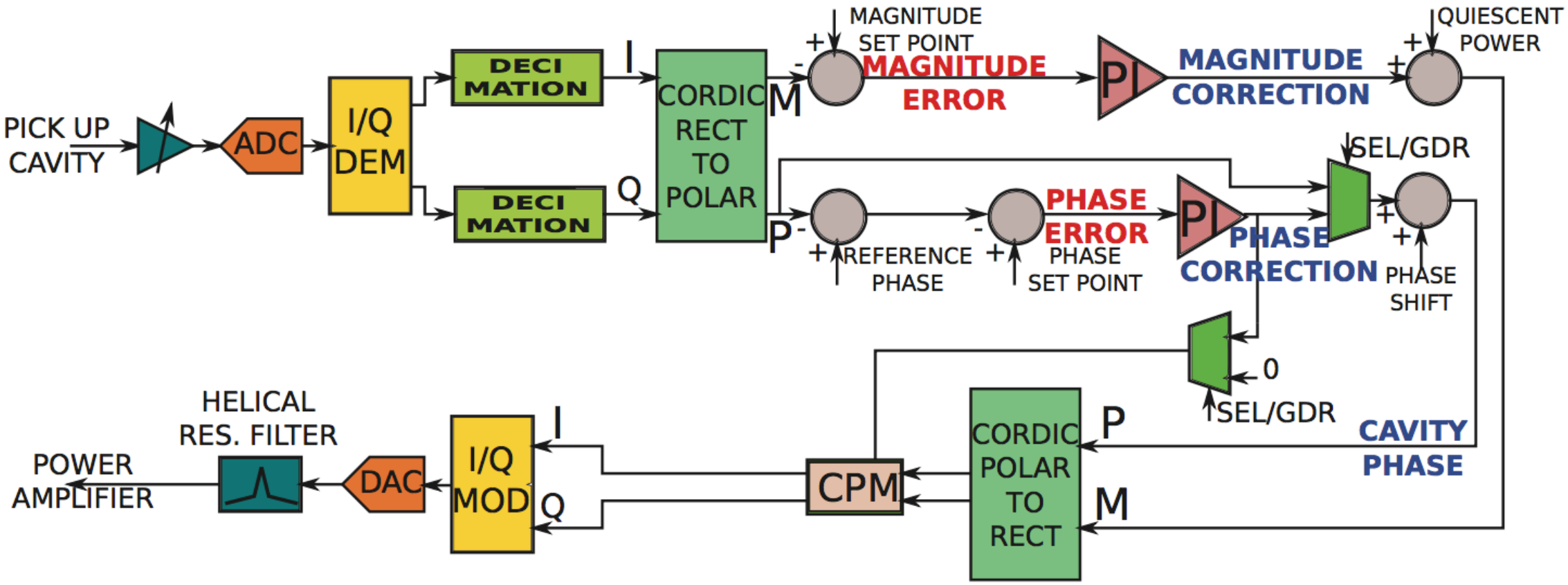
System block diagram

Adapt amplitude levels of RF signals

Measure reflected and forward powers



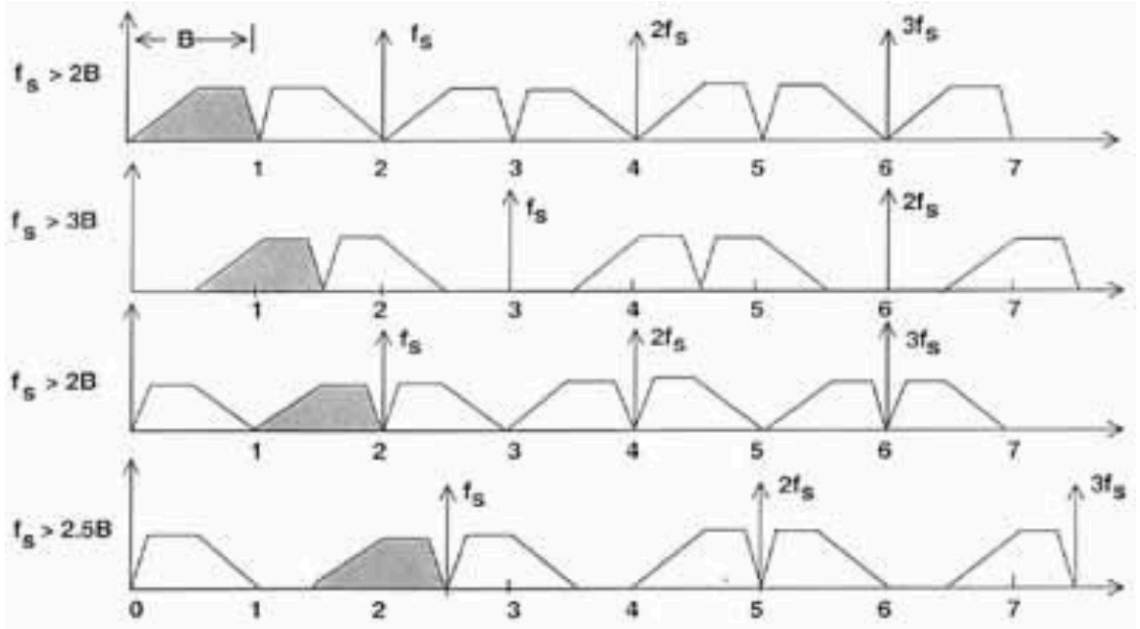
Algorithm block diagram

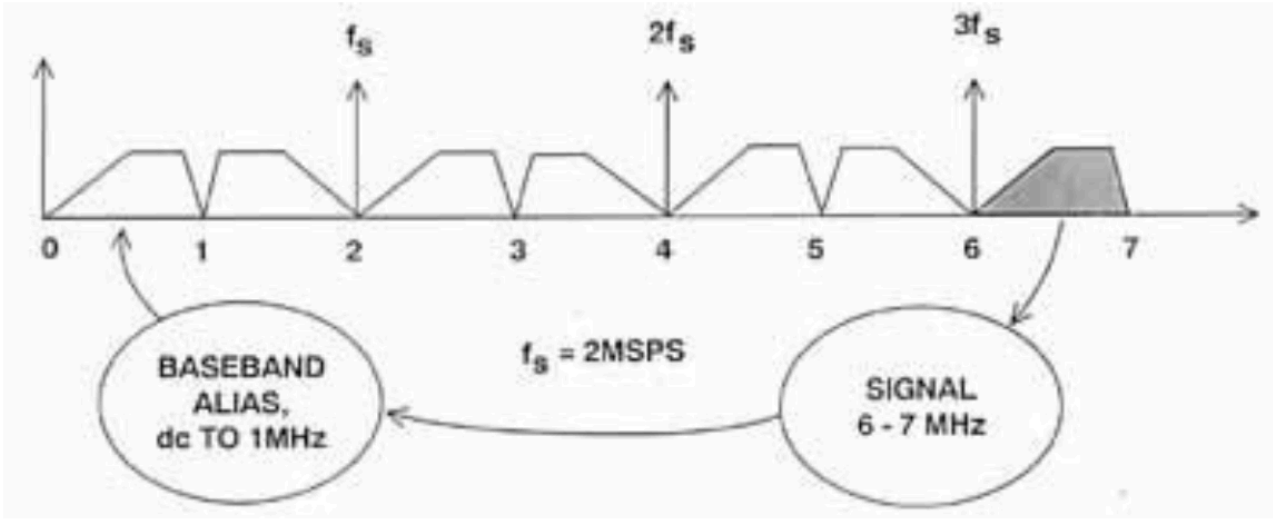


RF ADCs

- ADS42JB69, 16 bit, 250 MSPS
- Undersampling at 121.9 MHz

$$f_{RF} = \frac{1}{D}\left(kf_s \pm \frac{f_s}{4}\right), \forall k \in Z | k \geq 1 \qquad f_s \geq 4B$$





- Noise is dominated by clock jitter

$$SNR = -20log(2\pi f t_j)$$

16 bit ADC SNR_{max} = 98dB
tj_{min} ~ 0.016 ps
10 bit -> 62dB -> ~1.04 ps

DEVELOPMENT OF 200 MHz DIGITAL LLRF SYSTEM FOR THE 1 MeV/n RFQ AT KOMAC*

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Abstract

As a part of the R&D towards the multi-purpose ion irradiation system, 1 MeV/n RFQ will be developed at KOMAC (Korea Multi-purpose Accelerator Complex). This paper presents the latest Low Level RF (LLRF) test results obtained with 200 MHz dummy cavity. The main focus will be on the programmed FPGA (Field Programmable Gate Array) control logics using the PENTEK7156 based system [1]. Details about the firmware upgrades and future works will be described.

INTRODUCTION

The KOMAC multi-purpose ion irradiation system will include 200 MHz RFQ cavity. This RFQ system requires 1 % amplitude error stability. This RF system controlled through a digital LLRF board and the RF signal amplified with the SSA (Solid State Amplifier) as shown in the Fig. 1. The proposed LLRF system is controlled by only digital control board and samples the RF signal using

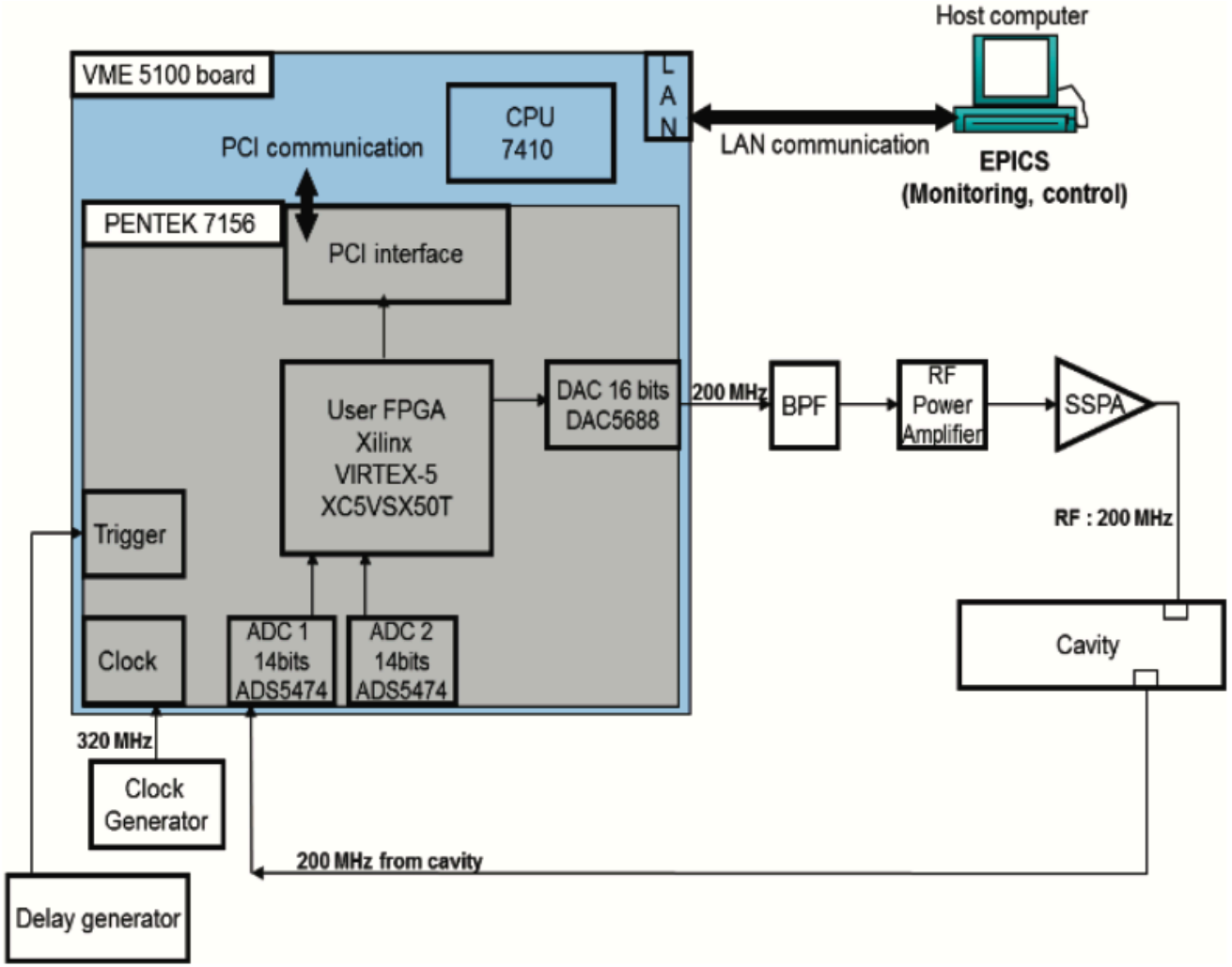
uses the VME5100 board and EPICS system to monitor and control the LLRF system. The output RF signal will be amplified by the SSA to supply the sufficient power RF signal to the RFQ cavity.

Figure 2: Digital LLRF PMC board and VME board.

Direct Sampling

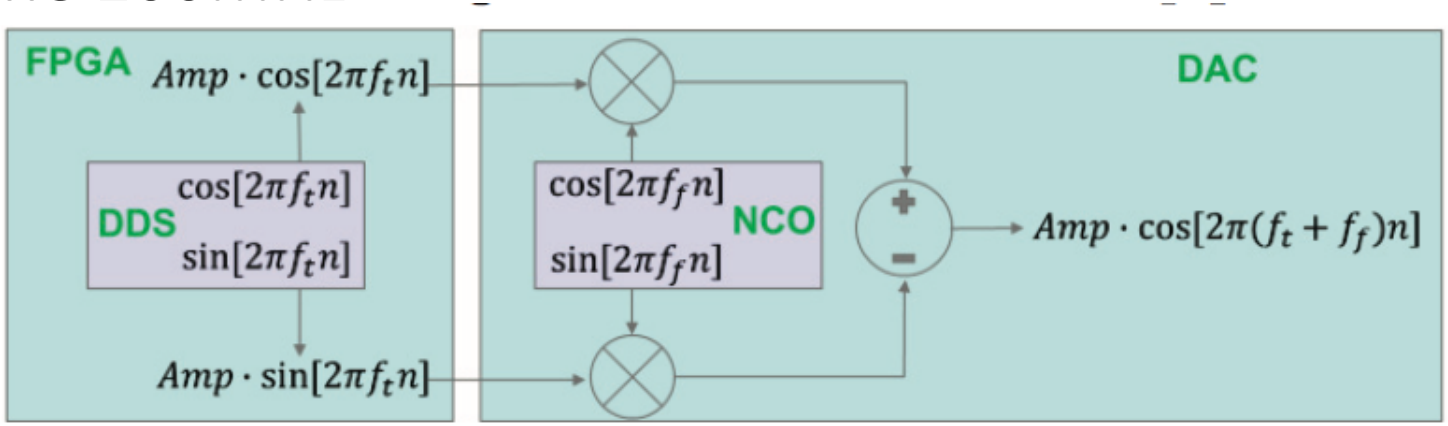
To minimize the analog components especially analog mixers, this system adopted the direct sampling. The

System block diagram

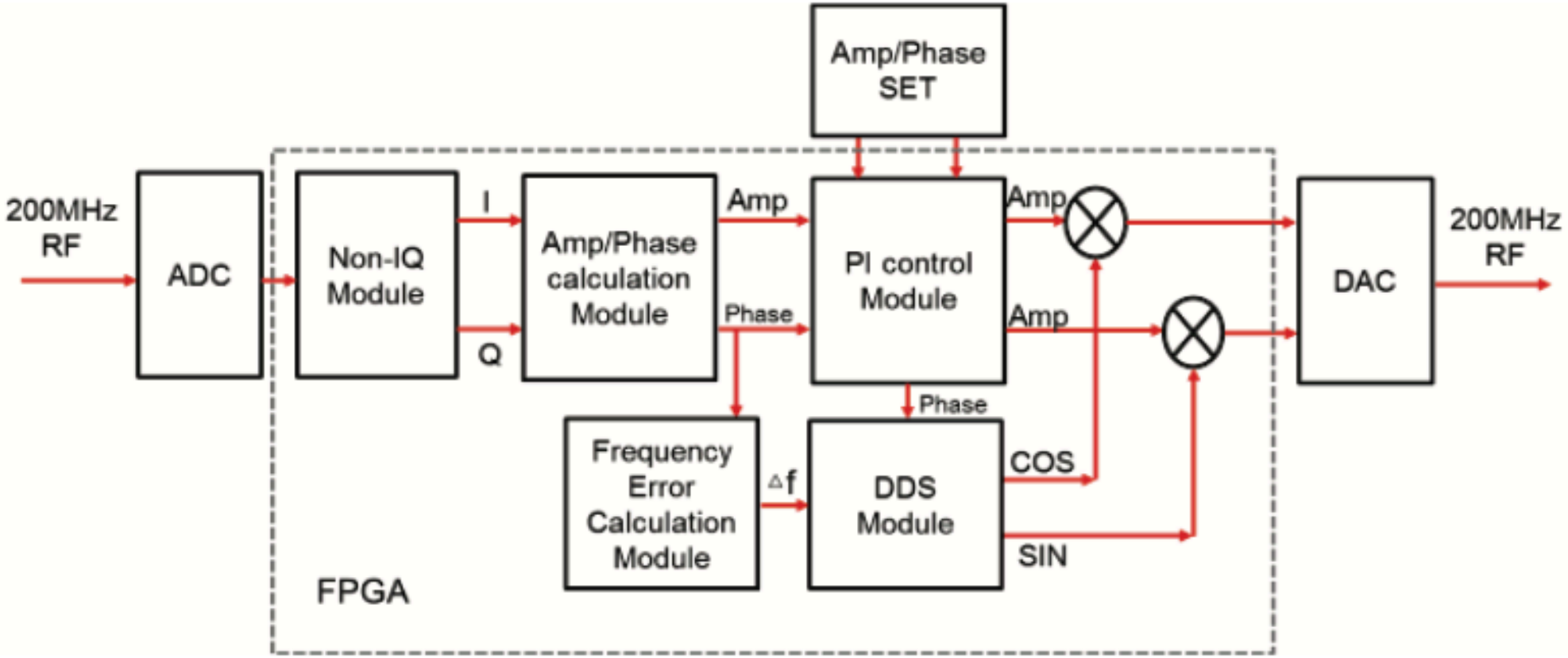


RF DACs

- 200 MHz signal
- Direct Digital Synthetizer (FPGA) generates 40 MHz
- Numerical Controlled Oscillator (DAC) generates 160MHz
- DAC acts as Digital Up Converter mixing the 40MHz and 160MHz to produce the 200MHz



Algorithm block diagram

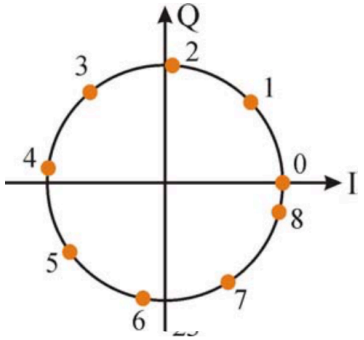


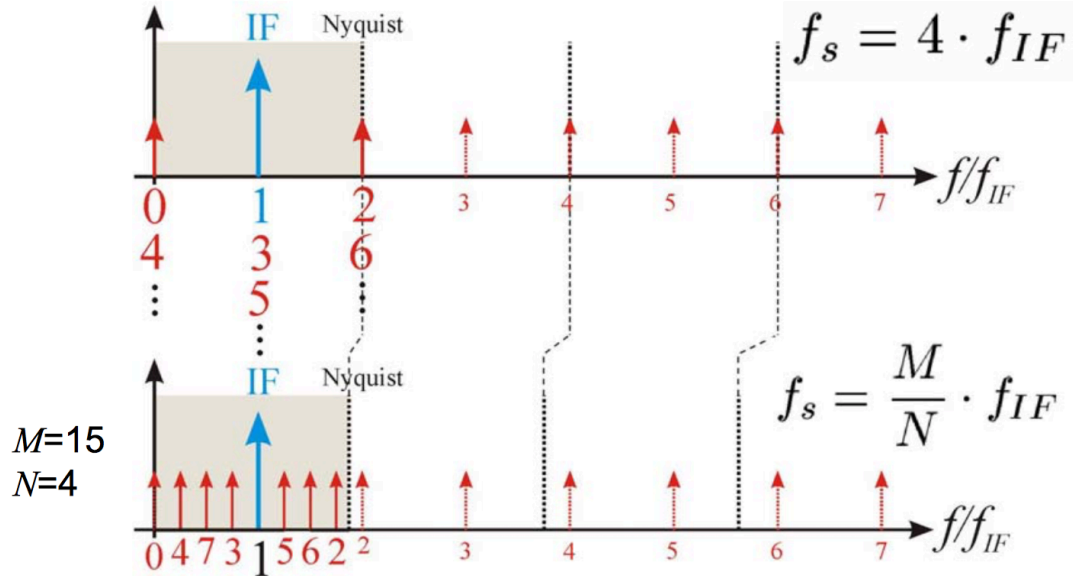
Non-IQ sampling

- The sampling frequency is
  - N samples in M IF periods

$$f_s = \frac{N}{M} \cdot f_{IF}$$

  - Example M=3, N=25





  - errors from DC offsets, clock jitter, ADC quantization, noise reduced
  - but more latency due to sampling *M IF* periods