Digital Signal Processing in RF Applications

Part I

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What are RF applications?

- any application which measures properties of an RF field
  (amplitude, phase, frequency, …);
  typical frequencies in accelerators: MHz – tens of GHz

- applications which process the measured quantities to control and regulate RF fields
  (feedback and feedforward)

Typical RF applications

Accelerators:

- CW / pulsed machines
- linear / circular machines
- electron/hadron/ion accelerators
- normal-/superconducting RF systems

Application areas (examples):

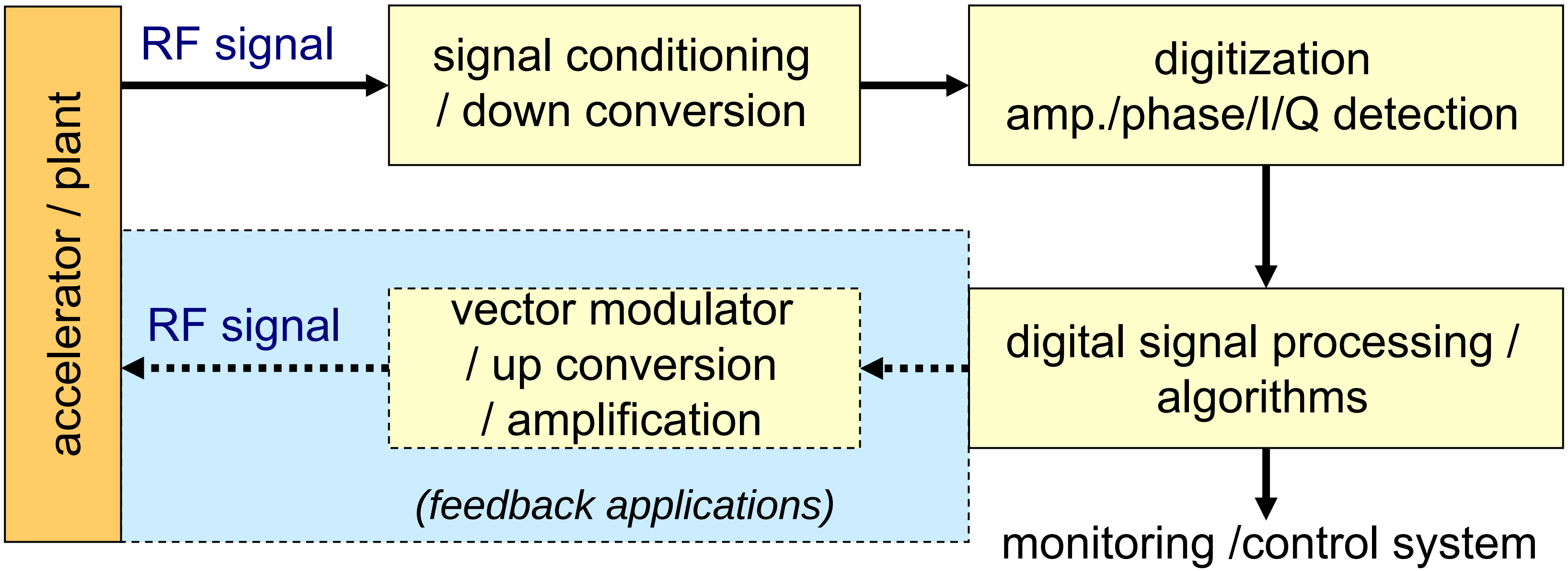
- cavity field loops (amplitude and phase)
- klystron loops (amplitude and phase)
- tuner loops (cavity tuning)
- radial and phase loops (circular machines)
- “RF gymnastics” (bunch splitting and merging)

Why digital RF applications?

	Digital	Analogue
Implementation	Learning curve + s/w effort	Easier/known ☺
Latency	Longer	Short ☺
DAQ/control	I/Q sampling (also direct) or DDC	Ampli/phase , IF downconversion
Algorithms	Sophisticated. ☺ State machines, exception handling...	Simple. Linear, time-invariant (ex: PID)
Multi-user	Full ☺	Limited
Remote control & diagnostics	Easy, often no additional h/w ☺	Difficult, extra h/w
Flexibility / reconfigurability	High (easier upgrades) ☺	Limited
Drift/tolerance	No drifts, repeatability ☺	Drift (temperature..), components tolerance
Transport distance without distortion	Longer ☺	Short
Radiation sensitivity	High	Small ☺

M. E. Angoletta "Digital LLRF" *EPAC'06*

Key components of digital RF applications

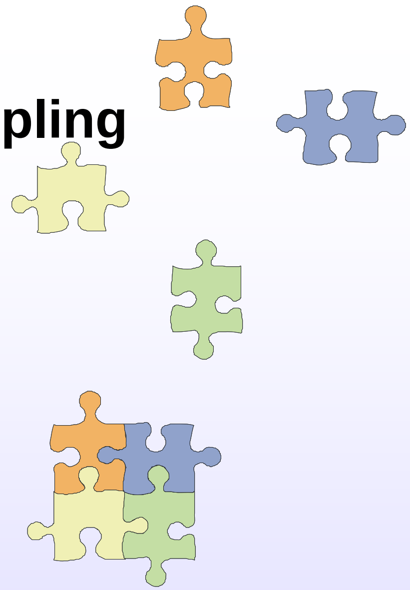


LLRF looks very similar to many other applications,
e.g. diagnostics (bunch-by-bunch feedback, position monitoring, …)

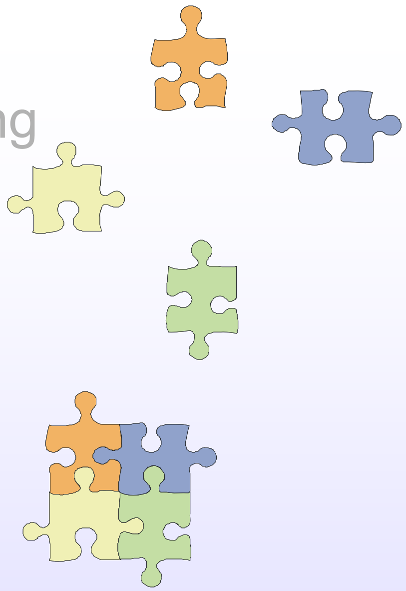
for feedback systems: ultimate error is dominated by the measurement process
(systematic error, accuracy, linearity, repeatability, stability, resolution, noise)

Outline

1. **signal conditioning / down conversion**
2. **detection of amp./phase by digital I/Q sampling**
   - I/Q sampling
   - non I/Q sampling
   - digital down conversion (DDC)
3. **upconversion**
4. **algorithms in RF applications**
   - feedback systems
   - adaptive feed forward
   - system identification



Outline



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Signal conditioning / down conversion

Why down conversion of the RF signal?

- ADC speeds are limited.
  It is not reasonable/possible today to digitize high-frequency carriers directly. (f>500 MHz)

- ADC dynamic range is limited.

  10 bit → 60 dB
  12 bit → 72 dB
  14 bit → 84 dB

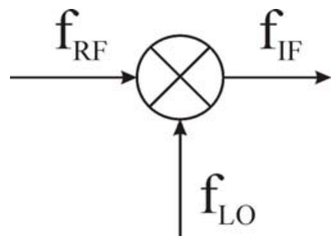
  ➡ often better: use analogue circuits in conjunction with the ADC to implement automated gain control (AGC) functions to ensure that this range is best used

- ADC clock and aperture jitter become critical at high frequencies (especially for undersampling schemes)

➡ **RF mixers are essential for digital high frequency applications**

RF mixer (ideal)

$$y_{RF}(t) = A_{RF} \cdot \sin(\omega_{RF} t + \varphi_{RF})$$



$$y_{IF}(t) = y_{RF}(t) \cdot y_{LO}(t)$$

$$y_{LO}(t) = A_{LO} \cdot \cos(\omega_{LO} t + \varphi_{LO})$$

mixer: linear time varying circuit, non-linear circuit (diodes…)

$$\Rightarrow y_{IF}(t) = \frac{1}{2} A_{LO} A_{RF} \cdot \Big(\boxed{\sin[(\omega_{RF} - \omega_{LO})\,t + (\varphi_{RF} - \varphi_{LO})]} + \boxed{\sin[(\omega_{RF} + \omega_{LO})\,t + (\varphi_{RF} + \varphi_{LO})]} \Big)$$

lower sideband

upper sideband

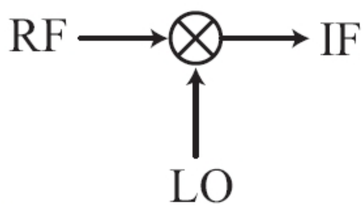
➡ even ideal mixers produce two sidebands

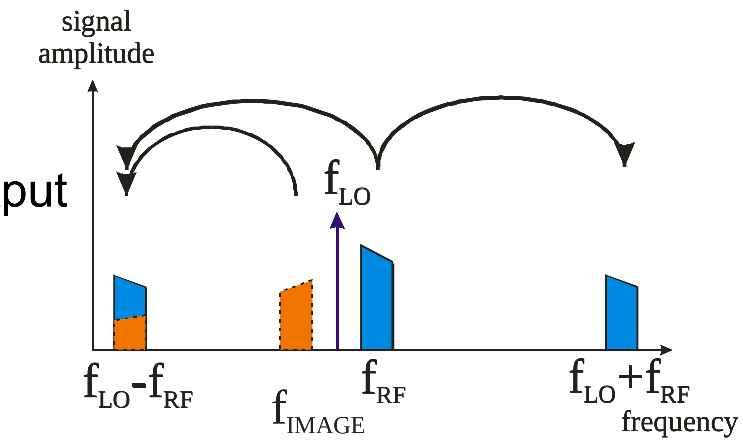
RF mixer (ideal)

- ideal mixer: output is the multiplication of the two input signals
- down conversion:

  RF, LO are high frequency inputs

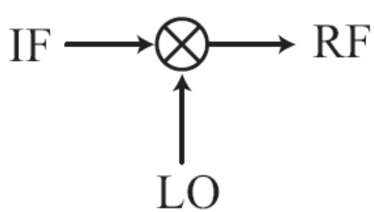
  IF: lower intermediate frequency output

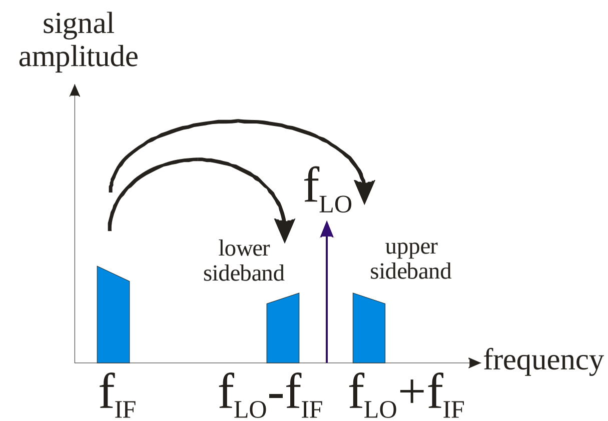




- up conversion:

  IF is input, RF is output





RF mixer (ideal)

down conversion:

$$y_{IF}(t) = \frac{1}{2} A_{LO} A_{RF} \cdot \left(\sin\left[(\omega_{RF} - \omega_{LO})\,t + (\varphi_{RF} - \varphi_{LO})\right] + \sin\left[(\omega_{RF} + \omega_{LO})\,t + (\varphi_{RF} + \varphi_{LO})\right] \right)$$

low pass filtering the upper sideband:

$$\boxed{\Rightarrow y_{IF}(t) = A_{IF} \cdot \sin\left(\omega_{IF} t + \varphi_{IF} \right)}$$

$$\begin{array}{lclccl} \omega_{IF} & = & \omega_{RF} - \omega_{LO} & & & \\ A_{IF} & = & \frac{1}{2} A_{LO} A_{RF} & \sim & A_{RF} & \text{with constant } A_{LO} \\ \varphi_{IF} & = & \varphi_{RF} - \varphi_{LO} & \sim & \varphi_{RF} & \text{with constant } \varphi_{LO} \end{array} \Bigg\}$$

basic properties of RF signal are conserved (ampl./phase)

important properties:

- phase changes/jitter are conserved during down conversion, e.g. 1° @ f_{RF}=1.5 GHz ↔ 1° @ f_{IF}=50 MHz
- comparison: sampling IF or RF (direct sampling)? timing jitter results in different phases! (e.g. 10 ps @ 500 MHz → 1.8°; 10 ps @ 50 MHz → 0.18°)

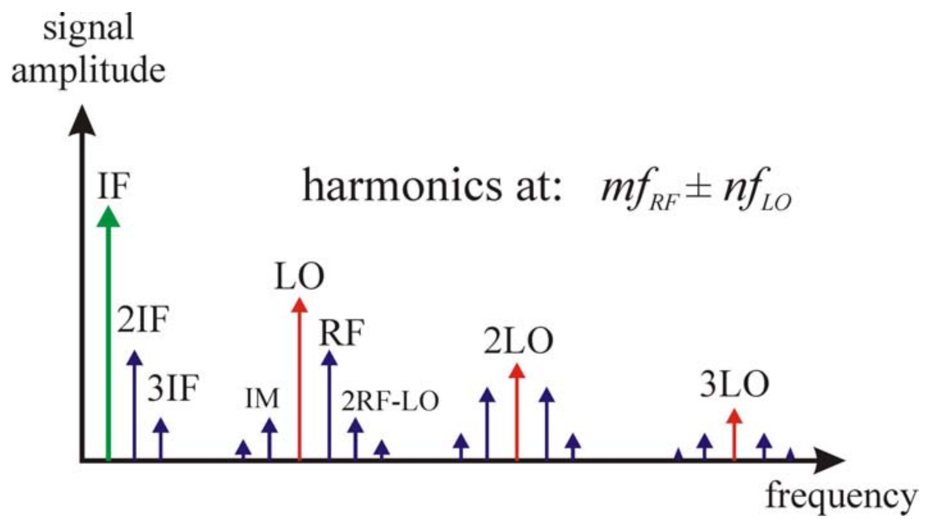
→ **tougher requirements for direct RF sampling !**

RF mixer (real)

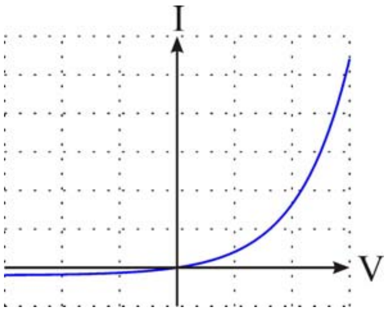
real mixers = non linear devices

➡ many undesired harmonics in frequency spectrum

➡ non-linearities in IF signal



I-V curve of a diode



$$I = I_0(e^{V/V_T} - 1)$$

$$\Delta I = I_0 e^{V/V_T}\left(\frac{\Delta V}{V_T} + \frac{1}{2}\left(\frac{\Delta V}{V_T}\right)^2 + \frac{1}{6}\left(\frac{\Delta V}{V_T}\right)^3 + \ldots\right)$$

➡ filtering the output of a mixer might be necessary

➡ take care about the introduced group delay by the filter

} trade off!

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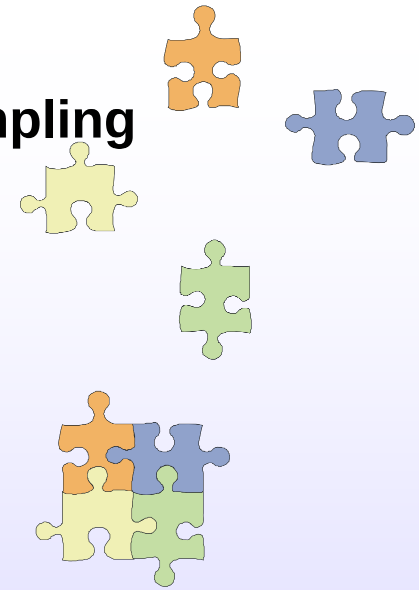
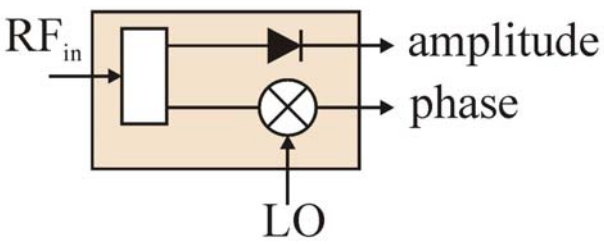
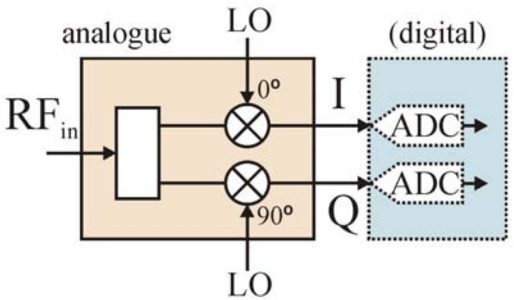


Amplitude and phase detection

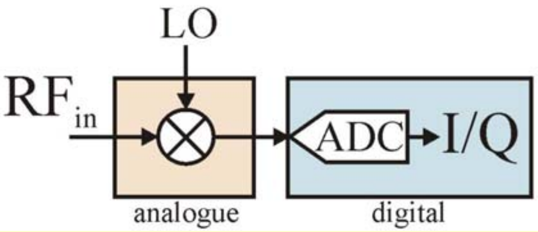
- direct amplitude phase detectors



- analogue IQ detection

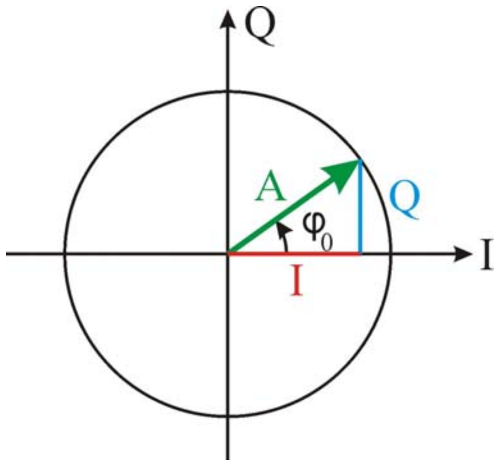


- digital IQ sampling /
  Digital Down Conversion (DDC)



RF vector representation

representation of any sinusoidal RF signal: phasor
(assumption: we measure the vertical component with ADC)



$$
\begin{aligned}
y(t) &= A \cdot \sin(\omega t + \varphi_0) \\
y(t) &= \underbrace{A \cos \varphi_0}_{=:I} \sin \omega t + \underbrace{A \sin \varphi_0}_{=:Q} \cos \omega t
\end{aligned}
$$

I: in-phase component

Q: quadrature-phase component

$$
\boxed{
\begin{aligned}
y(t) &= I \cdot \sin \omega t + Q \cdot \cos \omega t \\
I &= A \cdot \cos \varphi_0 \quad \Big| \quad A = \sqrt{I^2 + Q^2} \\
Q &= A \cdot \sin \varphi_0 \quad \Big| \quad \varphi_0 = \operatorname{atan}\left(\frac{Q}{I}\right)
\end{aligned}
}
$$

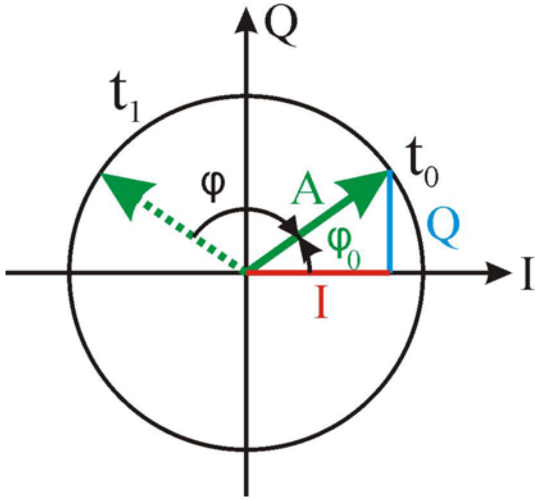
(sometimes I/Q are defined vice versa!)

definition:
positive frequencies
↔ counterclockwise rotating phasor

IQ sampling (1)

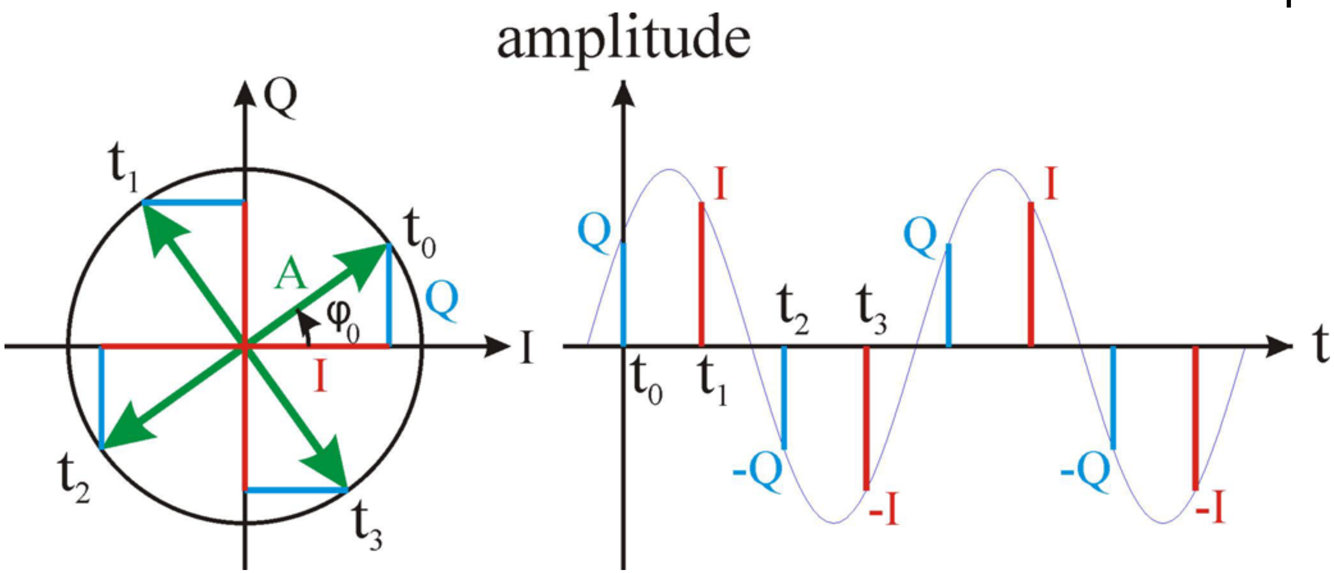
goal: monitor amplitude/phase (A/φ_0) variations of incoming RF/IF signal
➡ possible also to monitor I/Q at a reference time (reference phase)

➡ "process" sampled I/Q values for comparison,
i.e. rotate phasor back to reference phasor if phase advance between sampling is well known



IQ sampling (2)

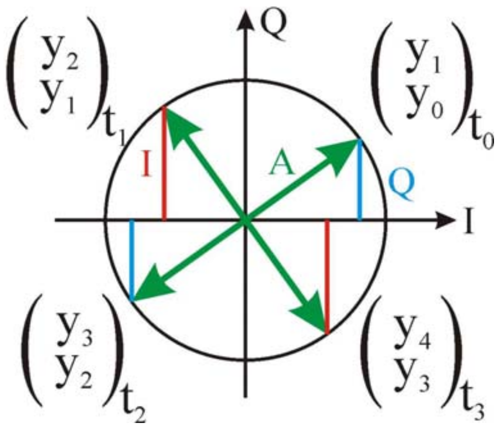
sampling of RF/IF freq.: $\boxed{f_s = 4 \cdot f}$ (i.e. 90° phase advance between two samples)



$$\left.\begin{aligned} y(t) &= I \cdot \sin \omega t + Q \cdot \cos \omega t \\ I &= A \cdot \cos \varphi_0 \\ Q &= A \cdot \sin \varphi_0 \end{aligned}\right\}$$

$$\begin{aligned} \omega t_0 &= 0: & y(t_0) &= Q \\ \omega t_1 &= \pi/2: & y(t_1) &= I \\ \omega t_2 &= \pi: & y(t_2) &= -Q \\ \omega t_3 &= 3\pi/2: & y(t_3) &= -I \end{aligned}$$

IQ sampling (3)



- build up I/Q vector based on two successive samples
- rotate corresponding I/Q vector by -90° / -180 ° / -270 ° in order to compare to initial I/Q values

$$
\begin{aligned}
y_0 &= y(t_0) = Q \\
y_1 &= y(t_1) = I \\
y_2 &= y(t_2) = -Q \\
y_3 &= y(t_3) = -I
\end{aligned}
$$

rotation matrix with angle $\Delta\varphi$:

$$
\begin{pmatrix} \cos\Delta\varphi & -\sin\Delta\varphi \\ \sin\Delta\varphi & \cos\Delta\varphi \end{pmatrix}
$$

$$t_0: \quad \begin{pmatrix} 1 & 0 \\ 0 & 1 \end{pmatrix} \cdot \begin{pmatrix} y_1 \\ y_0 \end{pmatrix} = \begin{pmatrix} y_1 \\ y_0 \end{pmatrix} = \begin{pmatrix} I \\ Q \end{pmatrix}_{t_0}$$

$$t_1: \quad \begin{pmatrix} 0 & 1 \\ -1 & 0 \end{pmatrix} \cdot \begin{pmatrix} y_2 \\ y_1 \end{pmatrix} = \begin{pmatrix} y_1 \\ -y_2 \end{pmatrix} = \begin{pmatrix} I \\ Q \end{pmatrix}_{t_1}$$

$$t_2: \quad \begin{pmatrix} -1 & 0 \\ 0 & -1 \end{pmatrix} \cdot \begin{pmatrix} y_3 \\ y_2 \end{pmatrix} = \begin{pmatrix} -y_3 \\ -y_2 \end{pmatrix} = \begin{pmatrix} I \\ Q \end{pmatrix}_{t_2}$$

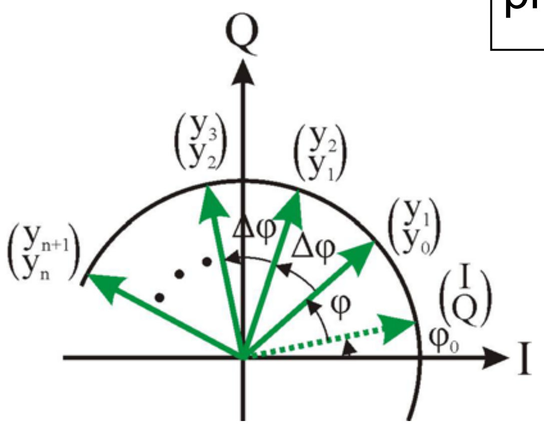
$$t_3: \quad \begin{pmatrix} 0 & -1 \\ 1 & 0 \end{pmatrix} \cdot \begin{pmatrix} y_4 \\ y_3 \end{pmatrix} = \begin{pmatrix} -y_3 \\ y_4 \end{pmatrix} = \begin{pmatrix} I \\ Q \end{pmatrix}_{t_3}$$

- I/Q processing with sampling frequency f_S

IQ sampling (4)

general: $f_s/f_{IF} = m, \qquad m:\text{integer}$

phase advance between consecutive samples: $\Delta\varphi = \frac{2\pi}{m}$



1. relation between measured amplitudes and I/Q

$$\begin{pmatrix} I_n \\ Q_n \end{pmatrix} = \frac{1}{\sin\Delta\varphi}\cdot\begin{pmatrix} 1 & -\cos\Delta\varphi \\ 0 & \sin\Delta\varphi \end{pmatrix}\cdot\begin{pmatrix} y_{n+1} \\ y_n \end{pmatrix}$$

2. rotation of $\binom{I_n}{Q_n}$ to $\binom{I_0}{Q_0} = \binom{y_1}{y_0}$ with angle $-n\Delta\varphi$:

$$\begin{pmatrix} I_0 \\ Q_0 \end{pmatrix} = \frac{1}{\sin\Delta\varphi}\cdot\begin{pmatrix} \cos n\Delta\varphi & -\cos(n+1)\Delta\varphi \\ -\sin n\Delta\varphi & \sin(n+1)\Delta\varphi \end{pmatrix}\cdot\begin{pmatrix} y_{n+1} \\ y_n \end{pmatrix}$$

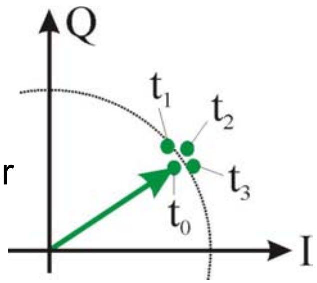
3. rotation of $\binom{I_0}{Q_0}$ to $\binom{I}{Q}$ with angle $-\varphi$:

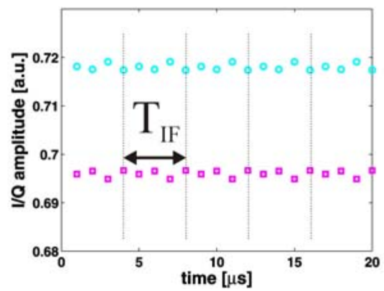
$$\boxed{\begin{pmatrix} I \\ Q \end{pmatrix} = \frac{1}{\sin\Delta\varphi}\cdot\begin{pmatrix} \cos(\varphi+n\Delta\varphi) & -\cos(\varphi+(n+1)\Delta\varphi) \\ -\sin(\varphi+n\Delta\varphi) & \sin(\varphi+(n+1)\Delta\varphi) \end{pmatrix}\cdot\begin{pmatrix} y_{n+1} \\ y_n \end{pmatrix}}$$

IQ sampling – potential problems (1)

- DC offsets of carrier frequency
- samples are not exactly 90° apart
  (e.g. due to ADC clock jitter)
  ➡ ripple on I/Q values with freq. of carrier (e.g. f_{IF})

rotated vector





- choosing phase advances "far" away from 90° can worsen signal to noise ratio

$$\begin{pmatrix} I_0 \\ Q_0 \end{pmatrix} = \frac{1}{\sin\Delta\varphi} \cdot \begin{pmatrix} \cos n\Delta\varphi & -\cos(n+1)\Delta\varphi \\ -\sin n\Delta\varphi & \sin(n+1)\Delta\varphi \end{pmatrix} \cdot \begin{pmatrix} y_{n+1} \\ y_n \end{pmatrix}$$

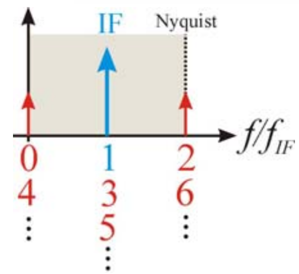
"easily" detectable errors in IQ demodulation

IQ sampling – potential problems (2)

- differential non-linearities of ADCs
- non-linearities of mixers

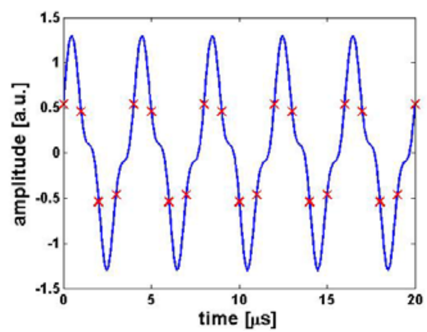
➡ generate high harmonics of input carrier
➡ odd harmonics of carrier frequency are not distinguishable from carrier by IQ detection

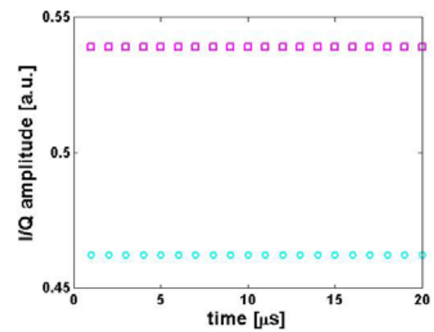
$$f_s = 4 \cdot f_{IF}$$



errors difficult to detect in IQ demodulation

example:
IF fundamental with 20% of 3rd harmonic component





➡ if input phase and amplitude changes, the distortion changes and can corrupt the measurement

Non-IQ sampling

recall: $y(t) = I \cdot \sin \omega t + Q \cdot \cos \omega t$

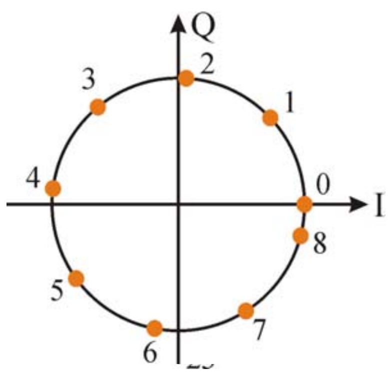
choose sampling frequency f_S and IF frequency f_{IF} such that:

$\boxed{N \cdot T_s = M \cdot T_{IF}}$ $f_s = \frac{N}{M} \cdot f_{IF}$ N, M: integers
N samples in M IF periods

➡ phase advance between two samples: $\Delta\varphi = \omega_{IF} T_s = 2\pi \frac{T_s}{T_{IF}} = 2\pi \frac{M}{N}$

➡ sampling "whole" IF sinusoidal signal if M, N are properly chosen

example: M=3 (IF periods), N=25



$$\begin{aligned}
y_0 &= I \cdot \sin \varphi_0 &&+ Q \cdot \cos \varphi_0 \\
y_1 &= I \cdot \sin \varphi_1 &&+ Q \cdot \cos \varphi_1 \\
y_2 &= I \cdot \sin \varphi_2 &&+ Q \cdot \cos \varphi_2 \\
&\dots \\
y_{(N-1)} &= I \cdot \sin \varphi_{(N-1)} &&+ Q \cdot \cos \varphi_{(N-1)}
\end{aligned}$$

where $\varphi_i = i \cdot \Delta\varphi = i \cdot 2\pi \frac{M}{N}$

➡ overestimated system of linear equations

➡ can be solved by least mean square algorithm

Non-IQ sampling (2)

least mean square algorithm:
minimize with respect to I,Q

$$f(I,Q) = \sum_{i=0}^{N-1} (I \cdot \sin\varphi_i + Q \cdot \cos\varphi_i - y_i)^2$$

$$\frac{\partial f}{\partial I} = 0, \qquad \frac{\partial f}{\partial Q} = 0$$

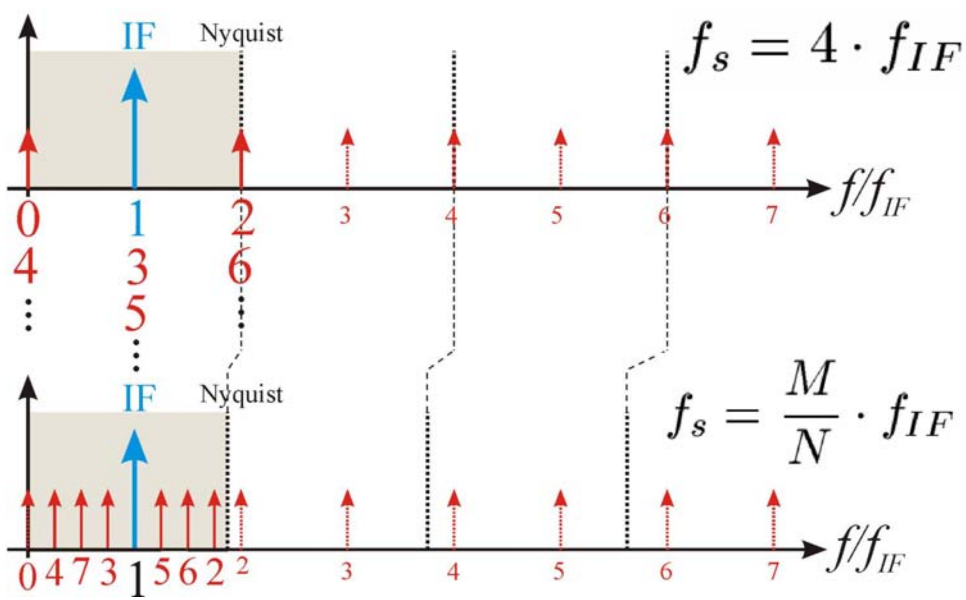
$$\Rightarrow \boxed{\begin{aligned} I &= \frac{2}{N} \cdot \sum_{i=0}^{N-1} y_i \cdot \sin(i \cdot \Delta\varphi) \\ Q &= \frac{2}{N} \cdot \sum_{i=0}^{N-1} y_i \cdot \cos(i \cdot \Delta\varphi) \end{aligned}}$$

if $N \cdot T_s = M \cdot T_{IF}$
(sin and cos can be pre-calculated and stored in look-up tables)

$$\varphi_i = i \cdot \Delta\varphi = i \cdot 2\pi \frac{M}{N}$$

Non-IQ sampling (3)

aliasing of harmonics:



M=15
N=4

most harmonics no longer line up with IF signal !

- errors from DC offsets, clock jitter, ADC quantization, noise reduced
- but more latency due to sampling M IF periods
- trade-off between noise reduction and linearity improvement and low latency

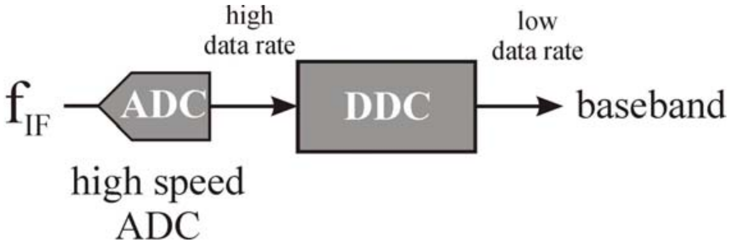
⟶ choose M,N properly !

Digital Down Conversion (DDC)

(sometimes referred to as "Digital Drop Receiver" (DDR))

Goal: shift the digitized band limited RF or IF signal from its carrier down to baseband

example: $f_{IF} = 40$ MHz
$f_S = 100$ MHz **(oversampling)**
signal BW = 1 MHz
➡ **output sample rate of 2.5 MHz is fine!**



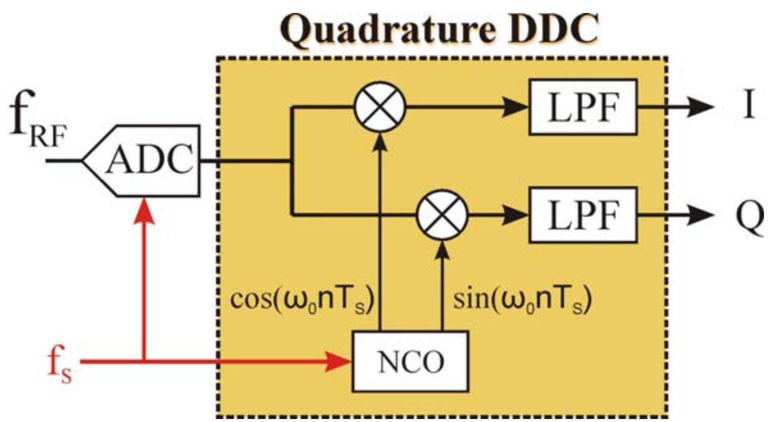
- reduce the amount of required subsequent processing of the signal without loss of any of the information carried by the IF signal

➡ **filtering and data reduction !**

- implementation on FPGA, DSP or ASIC
- two classes of DDCs:
  - narrowband (decimation R≥32, → CIC filter [Cascaded Integrator Comb])
  - wideband (decimation R<32, → FIR / multi-rate FIR filters)

DDC (2)

inside DDC: three major sections

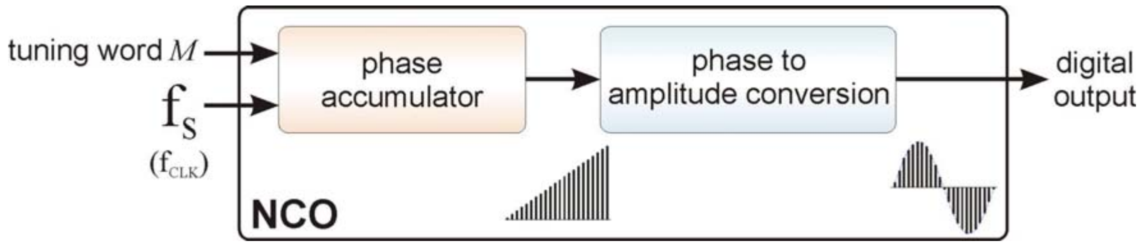


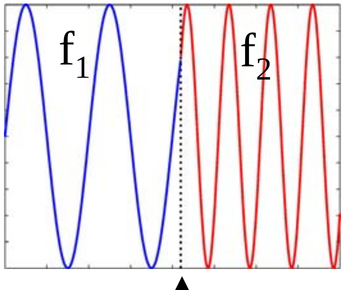
- **Local Oscillator** (Numerical Controlled Oscillator, NCO)
- **Mixer** (digital)
- **Decimating Low Pass Filter** (LPF)

DDC building blocks:

- NCO: direct digital frequency synthesizer (DDS)
  sine and cosine lookup table
- digital mixers: “ideal” multipliers → two output frequencies
  (sum and difference freq. signals)
- decimating low pass (anti alias) filter (often implemented as CIC and FIR)

DDC building block: NCO





new freq.

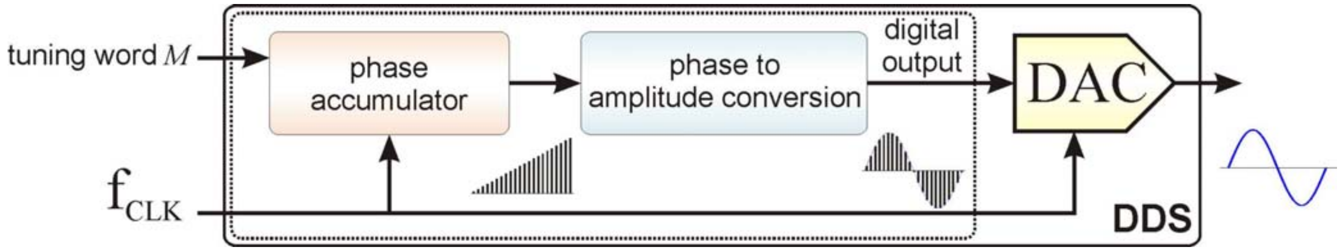
NCO functionality:

- **phase accumulator** → calculate new phase @ f_S with phase advance defined by tuning word. (NCO clock: sample rate f_S)
- **convert phase to amplitude**
(often done in ROM based sine lookup tables; either one full sin wave is stored or only a quarter with some math on the pointer increment)
- phase accumulator overflow → wrap around in circular lookup table

NCO advantages:

- tuning word is programmable
➡ frequencies up to nearly $f_S/2$ (Nyquist) possible
- extremely fast “hopping speed” in tuning output frequency, phase-continuous frequency hops with no over/undershoot or analog-related loop settling time anomalies.

addendum: Direct Digital Synthesis (DDS)



DDS properties:

- produce an analog waveform by generating a time-varying signal in digital form
- size of lookup table (phase to amp. conv.) is determined by:
  - number of table entries
  - bit width of entries (determines amplitude output resolution)
- output frequency: $$f_{out} = M \cdot \frac{f_{CLK}}{2^N}$$ (M: tuning word, N: length in bits of phase accumulator)

  example: N=32 bit ; f_S=50 MHz ➡ df= 12 mHz

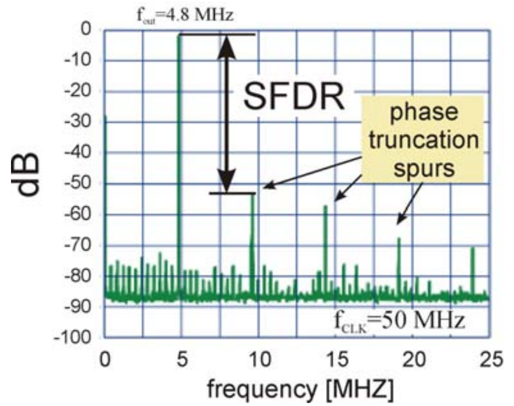
but: do we need 2^N (8 bit entries→ 4 GByte!) entries in lookup table?

Direct Digital Synthesis (2)

Phase truncation:

- in order to save memory in lookup table:
  → truncate phase before the lookup table!

  example: N=32: keep only upper most 12 bits, truncate lower 20 bits

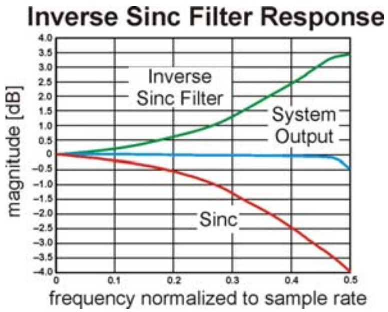


- implications:
  - introduce phase error which is periodic in time
  - result in amplitude errors during phase to amplitude conversion

→ **phase truncation spurs**

Output precompensation:

- sin(X)/X rolloff response due to DAC output spectrum which is quite significant
- precompensate output before DAC with inverse sinc filter

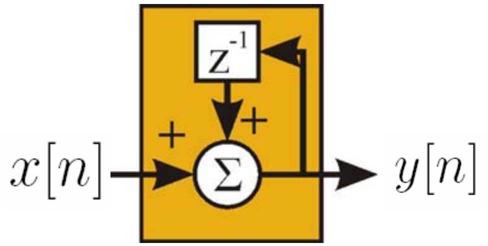


DDC building block:
Cascaded Integrator Comb Filter (CIC)

(introduced by Eugene Hogenauer, 1981)

- computationally efficient implementations of narrowband low pass filters (no multipliers needed!)
- multi-rate filter (decimation/interpolation)

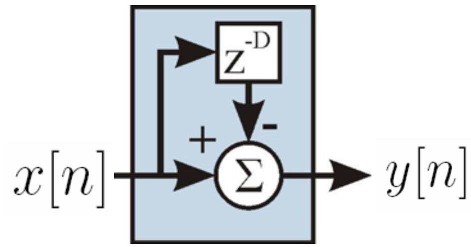
basic elements:



basic integrator

$$y[n] = y[n-1] + x[n]$$

$$\boxed{H_I(z) = \frac{1}{1 - z^{-1}}}$$



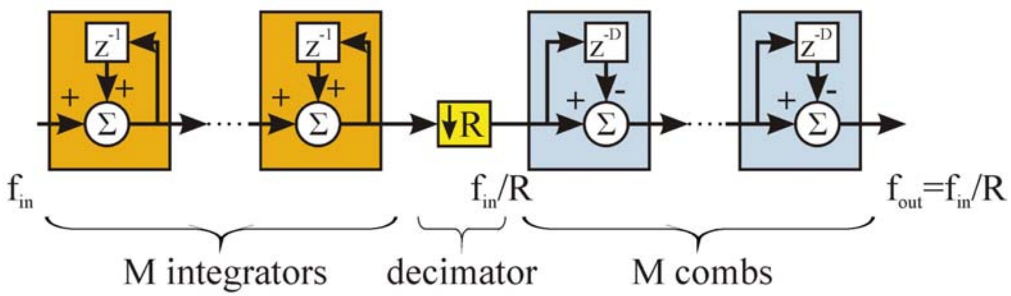
basic comb

$$y[n] = x[n] - x[n-D]$$

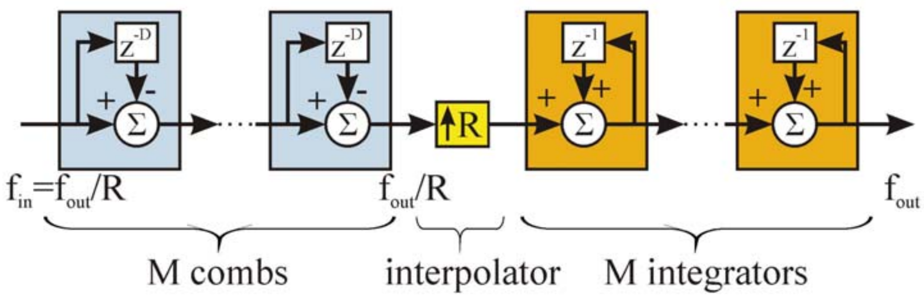
$$\boxed{H_C(z) = 1 - z^{-D}}$$

CIC filter (2)

filter structure for decimating CIC:



filter structure for interpolating CIC:



D: differential delay

reference sampling rate for transfer function: always higher freq.

➡ basic comb filter (referenced to the high input sample rate):

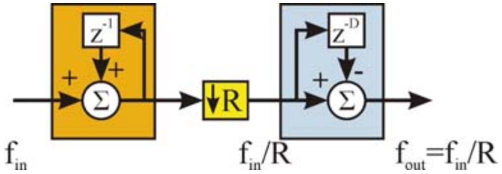
$$H_C(z) = 1 - z^{-RD}$$

$$\boxed{H(z) = (H_I)^M (H_C)^M = \frac{(1-z^{-RD})^M}{(1-z^{-1})^M} = \left(\sum_{k=0}^{RD-1} z^{-k}\right)^M}$$

FIR filter!
(stable)

How to understand CIC?

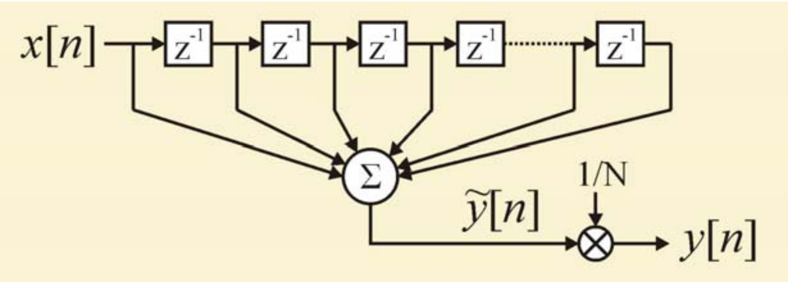
example: decimating CIC (1st order)
with integer decimation factor R



CIC: originate from the concept of a recursive running-sum filter
(efficient form of a non-recursive moving average filter [boxcar filter])

boxcar filter, length *N*:
(moving average)

$$y[n] = \frac{1}{N}\Big(x[n] + x[n-1] + \cdots + x[n-N+1]\Big)$$



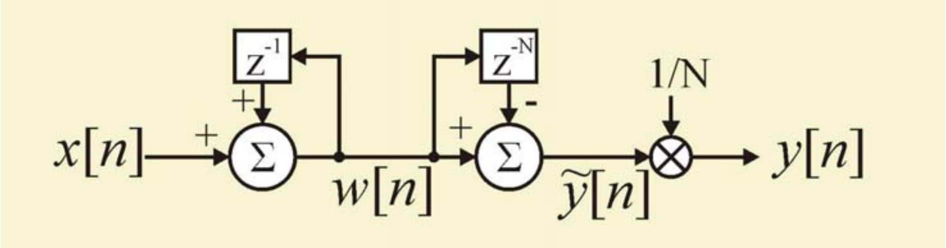
$$H(z) = \frac{1}{N}\Big(1 + z^{-1} + \cdots + z^{-(N-1)}\Big) = \frac{1}{N}\underbrace{\sum_{k=0}^{N-1} z^{-k}}_{\text{geometric sum}} = \frac{1}{N}\frac{1-z^{-N}}{1-z^{-1}}$$

How to understand CIC (2)

recursive running-sum:

$$y[n] = y[n-1] + \frac{1}{N}\Big(x[n] - x[n-N]\Big)$$

(alternate implementation of boxcar filter)



$$w[n] = z^{-1}w[n] + x[n]$$
$$y[n] = \frac{1}{N}\Big(w[n] + z^{-N}w[n]\Big)$$

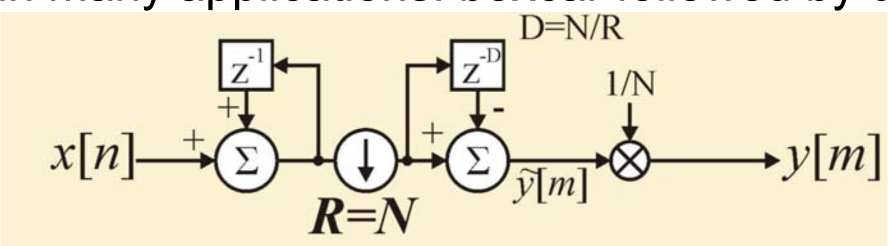
➡

transfer function:

$$H(z) = \frac{1}{N}\frac{1-z^{-N}}{1-z^{-1}}$$

in many applications: boxcar followed by decimation $R=N$

compare with 1^{st} order CIC:



$$H(z) = \frac{1}{N}\frac{1-z^{-RD}}{1-z^{-1}}$$

$$H(z) = \frac{1-z^{-RD}}{1-z^{-1}}$$

➡ **boxcar/recursive running-sum filters have the same transfer function as a 1^{st} order CIC (except: 1/N gain; general diff. delay D)**

CIC properties

- **applications:**
  - anti-aliasing filtering prior to decimation
  - typically employed in applications that have a large excess sample rate.
    → system sample rate is much larger than the bandwidth occupied by the signal
    (remember example: f_{IF} = 40 MHz, f_S = 100 MHz, signal BW = 1 MHz)
- **resources:** uses additions and subtractions only
- **frequency response:** evaluate $H(z)$ at $z = e^{i\omega T_S} = e^{i2\pi \frac{f}{f_S}}$

$$|H(e^{i\omega T_S})| = \left| \frac{\sin\left(\pi R D \frac{f}{f_S}\right)}{\sin\left(\pi \frac{f}{f_S}\right)} \right|^M$$

frequency response with respect to the output frequency $f_0 = \frac{f_S}{R}$

$$|H(f)| = \left| \frac{\sin\left(\pi D \frac{f}{f_0}\right)}{\sin\left(\frac{\pi}{R} \frac{f}{f_0}\right)} \right|^M$$

design parameter D determines locations of zeros:

$$f = k \cdot \frac{f_0}{D}$$ (k: integer)

CIC properties (2)

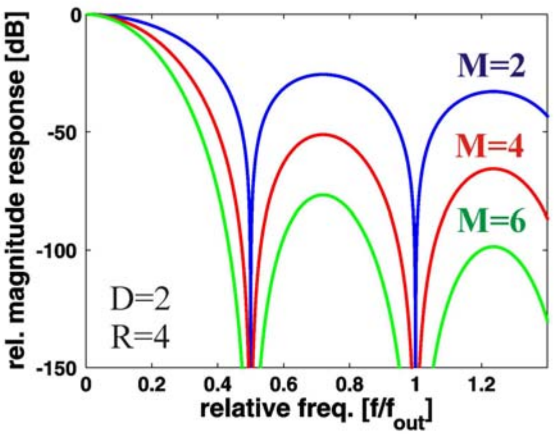
- **DC gain:**

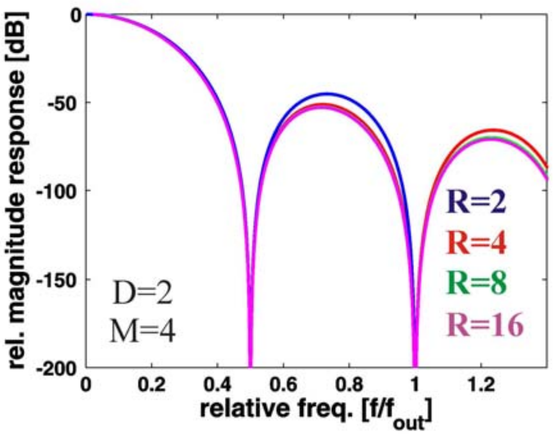
  net gain of CIC at DC: $(RD)^M$

  $$\lim_{f \to 0} |H(f)| = (RD)^M$$ ➡ plot relative freq. response $\frac{|H(f)|}{|H(0)|}$

  → Each additional integrator must add another bits width of (RD) for each stage (implementation with two's complement (nonsaturating) arithmetic due to overflows at each integrator)

- **frequency response:** (M: number of CIC stages, D: differential delay)



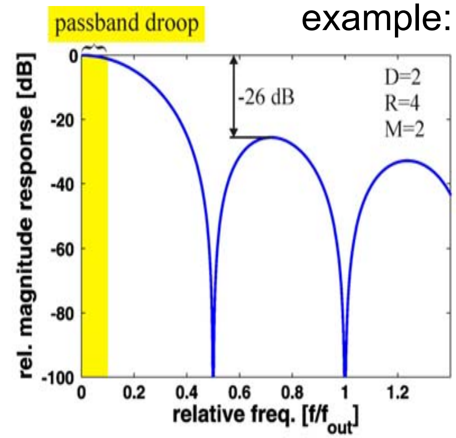


important characteristic:
shape of the filter response changes very little as a function of the decimation ratio R

CIC properties (3)

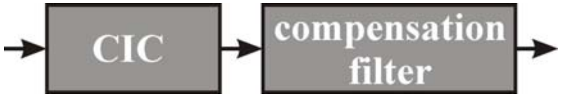
- to improve alias rejection
  → increase number of CIC stages (M)

  but:
  → this increases passband droop
  → droop is frequently corrected using an additional (non-CIC-based) stage of filtering

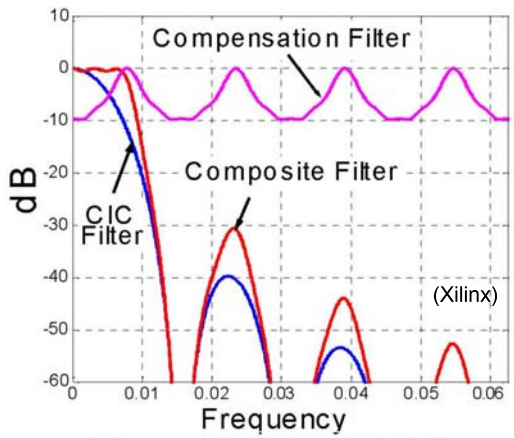


➡ compensation filter

(*decimator*: after CIC at reduced rate;



interpolator: precompensated before CIC)



CIC compensation filter for M = 3, R = 64.

DDC or IQ demodulation?

DDC

- long group delay
  (depending on clock speed and number of taps in the CIC/FIR filters)
- very flexible
  (NCO can follow f_{IF} over a broad range)
- data reduction and good S/N ratio

➔ applications with large varying IF, need for good S/N ration and reasonable latency

IQ demodulation

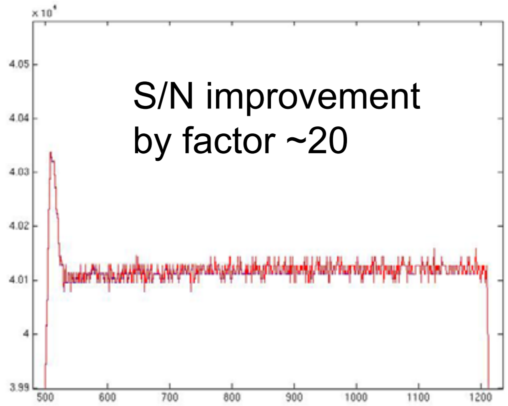
- low latency,
  simple implementation
- f_S is fixed to IF
- sensitive to clock jitter and non-linearities
- non-IQ sampling provides better S/N ratio on cost of latency

➔ feedback applications with fixed IF and ultra-short latency

Examples for DDC and IQ demodulation

DDC

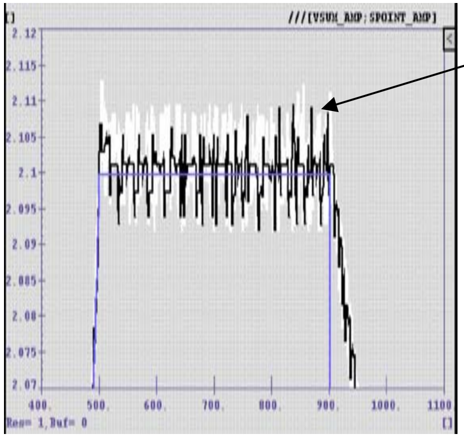
- super conducting cavity field (amplitude)



f_{IF}=13.54 MHz
f_S=54.17 MHz
f_{CLK}(FPGA)=75 MHz
5 stage CIC+ 21 tap FIR
delay: 25 clk cycles

IQ demodulation

- super conducting cavity field (amplitude)



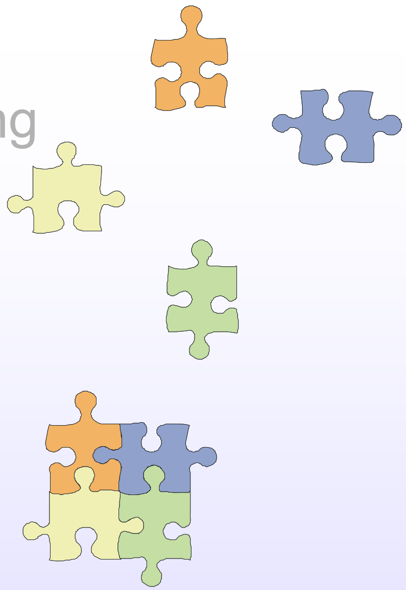
ripple:
250 kHz
IF freq.

f_{IF}=250 kHz
f_S=1 MHz
f_{CLK}(FPGA)=75 MHz
delay: 4 clk cycles

G. Castello
(FNAL)

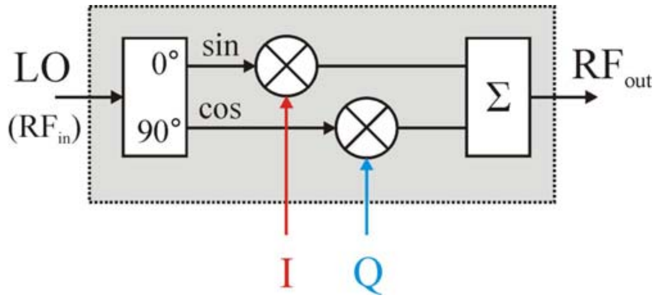
Outline

1. signal conditioning / down conversion
2. detection of amp./phase by digital I/Q sampling
   - I/Q sampling
   - non I/Q sampling
   - digital down conversion (DDC)
3. **upconversion**
4. algorithms in RF applications
   - feedback systems
   - adaptive feed forward
   - system identification



Up conversion – vector modulator

- RF signal: split into two branches, 90° phase shift (sin, cos)
- block diagram :



$$
\begin{aligned}
RF_{out}(t) &= I \cdot A_{RF} \cdot \sin \omega t + Q \cdot A_{RF} \cdot \cos \omega t \\
&= A_{out} \cdot \sin(\omega t + \varphi_0)
\end{aligned}
$$

$$A_{out} = A_{RF}\sqrt{I^2 + Q^2} \qquad \varphi_0 = \operatorname{atan}\left(\frac{Q}{I}\right)$$

- mixer operated as amplitude control elements
  ➡ any phase and amplitude of carrier can be generated

pure amplitude modulation:

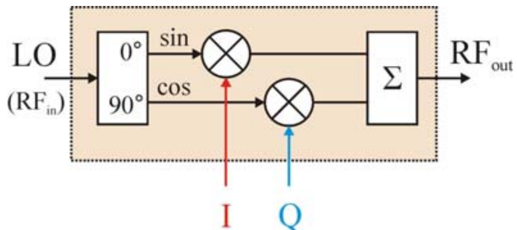
$$
\begin{aligned}
I(t) &= A_0(t) \cdot \cos \varphi_0 \\
Q(t) &= A_0(t) \cdot \sin \varphi_0
\end{aligned}
$$

pure phase modulation:

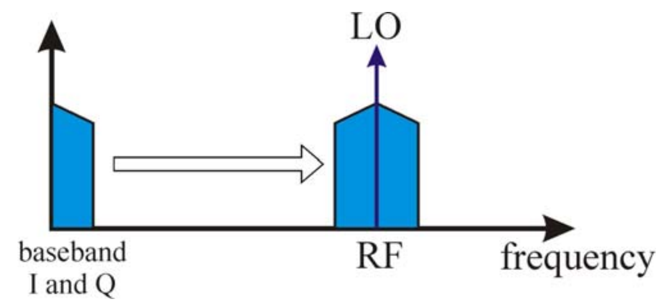
$$
\begin{aligned}
I(t) &= A_0 \cdot \cos \varphi_0(t) \\
Q(t) &= A_0 \cdot \sin \varphi_0(t)
\end{aligned}
$$

Vector modulator

- **homodyne upconversion** (direct upconverion, baseband upconversion):

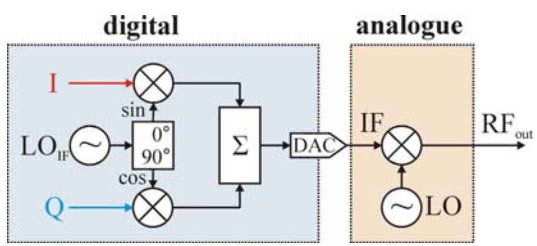


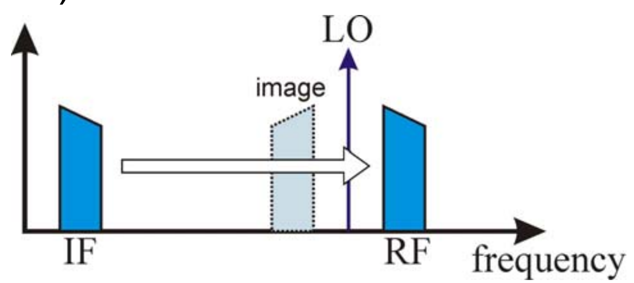
(analog/digital)



- **heterodyne upconversion** (IF upconversion)

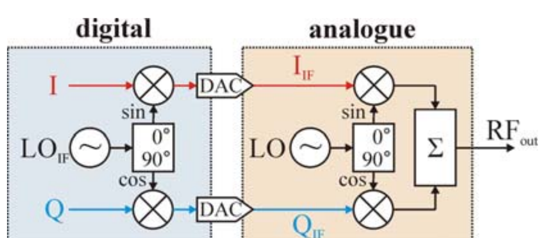
double sideband modulator

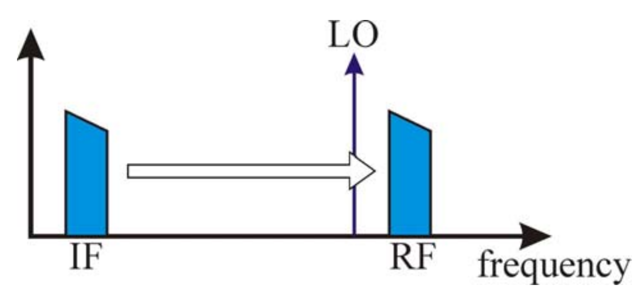




single sideband modulator

(phasing method)

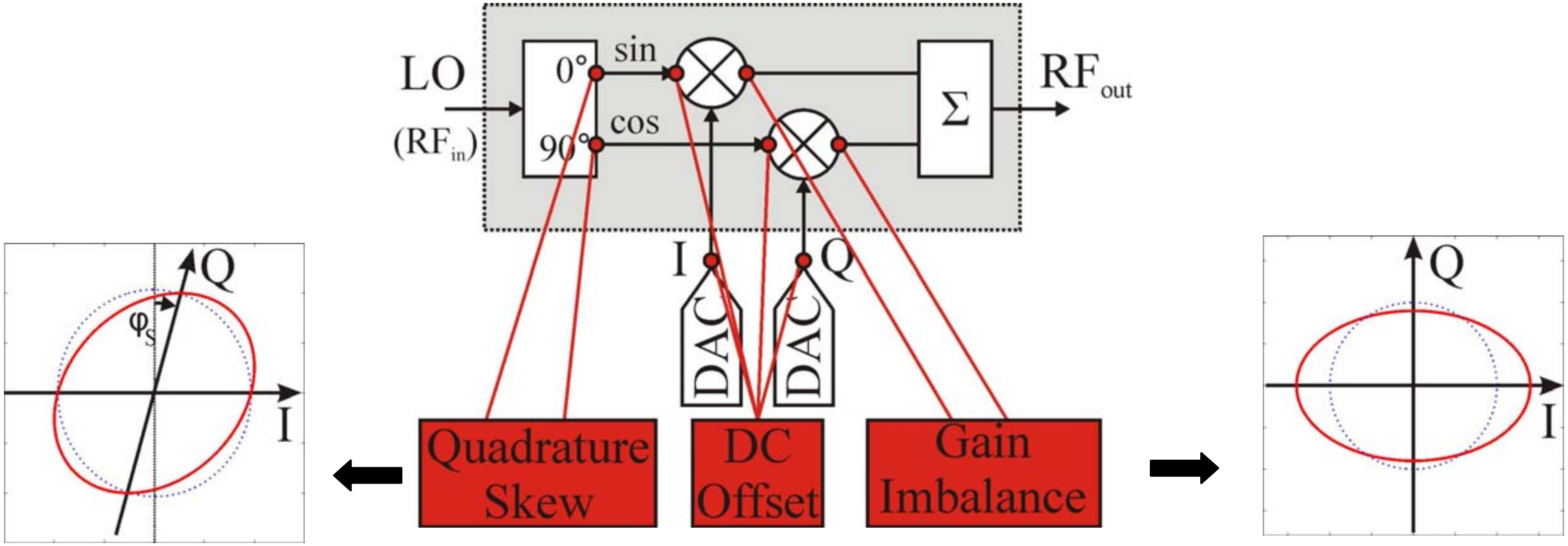




Vector modulator

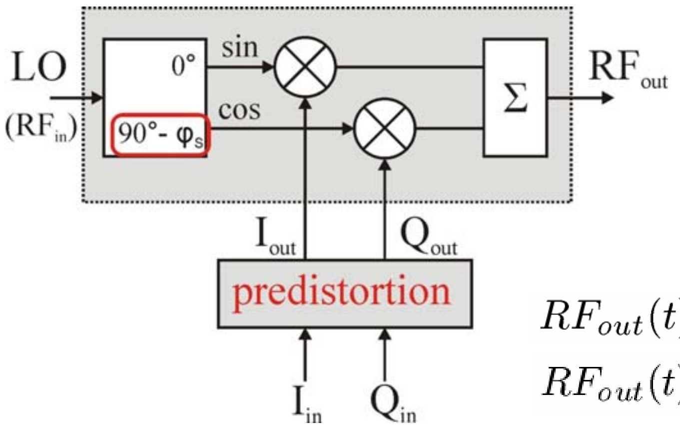
practical problems (homodyne vec. mod.): 1st order sources of errors

- offsets at mixer inputs ➡ carrier leakage
- two channels not exactly 90º apart ➡ I / Q skew
- gains of two RF paths and I/Q drives not exactly the same
  ➡ I / Q imbalance errors

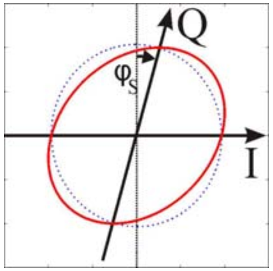


Vector modulator – digital predistortion

- **I/Q skew compensation**



φ_S : skew phase



RF output with skew:

$$RF_{out}(t) = I_{out} \cdot A_{RF} \cdot \sin \omega t + Q_{out} \cdot A_{RF} \cdot \cos(\omega t - \varphi_S)$$

$$RF_{out}(t) = (I_{out} + Q_{out} \sin \varphi_S) \cdot A_{RF} \sin \omega t + Q_{out} \cos \varphi_S \cdot A_{RF} \cos \omega t$$

predestortion of I/Q signal:

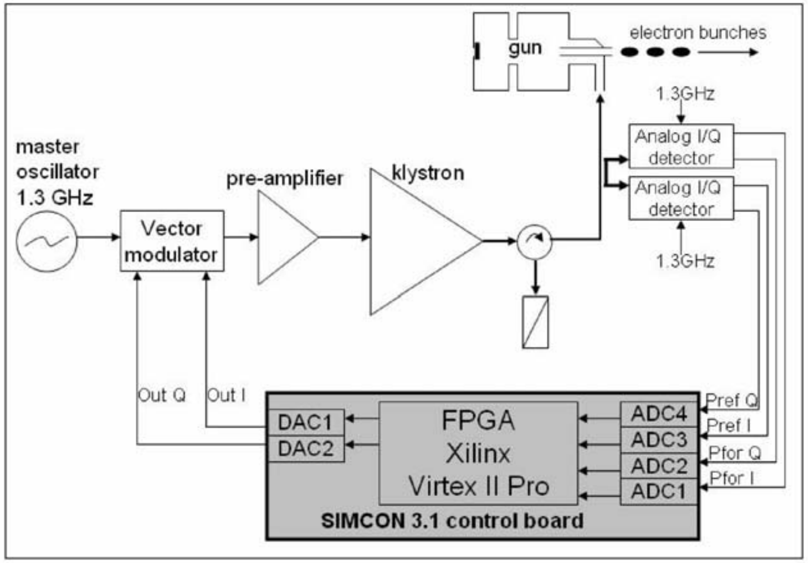
$$\boxed{\begin{pmatrix} I_{out} \\ Q_{out} \end{pmatrix} = \frac{1}{\cos \varphi_S} \cdot \begin{pmatrix} \cos \varphi_S & -\sin \varphi_S \\ 0 & 1 \end{pmatrix} \cdot \begin{pmatrix} I_{in} \\ Q_{in} \end{pmatrix}}$$

- **gain/offset compensation**
  define individual gain scaling factors and offset compensation constants for I/Q; pre-scale I/Q digitally before applying to vector modulator

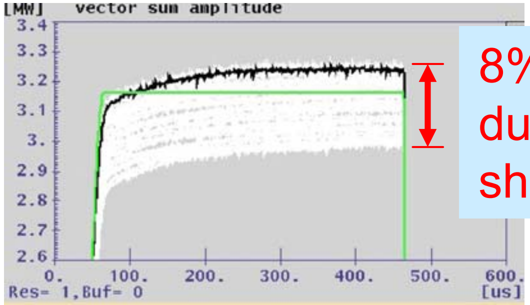
Vector modulator – digital predistortion (2)

- example of I/Q skew compensation: **RF gun control for FLASH**
  boundary condition: no field probe to detect field in RF cavity
  predistortion: adjust for skew and for gain imbalance

setup:

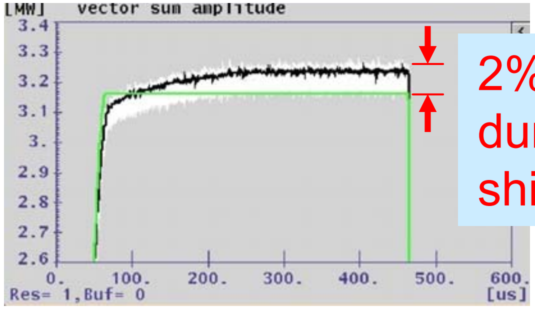


before vec. mod. linearization:



8% variation during phase shifts of 360°

after vec. mod. linearization:



2% variation during phase shifts of 360°

W. Koprek (DESY)